SEMICON EUROPA OCT 25–27, 2016 GRENOBLE, FRANCE CONNECT

Lithography

L. PAIN
Program Manager
CEA-LETI, DTSI, Grenoble, France

Biography
Laurent Pain is graduated from the Ecole Nationale Supérieure de Physique de Grenoble in 1992. He received his Ph D after his work on DUV resists study. He joined CEA-LETI in 1996 to work on infra-red technology, and then came back to microelectronics in 1999 working on 193nm and e-beam lithography technologies.
From 2008 to 2014, Laurent Pain leaded the lithography laboratory of the silicon technology division of CEA-LETI. He was also managing in parallel the industrial consortium IMAGINE dedicated to the development of multibeam lithography with MAPPER lithography BV.
Within the LETI Silicon Technology Division, he is now the manager of Patterning Programs including the business development around this activity.

EUV lithography industry status: progress and challenges

E. Hendrickx
Program manager
imec, Advanced Patterning, Leuven, Belgium

Abstract
EUV lithography has seen rapid progress over the last 2 years. The first ASML NXE:3300 production tools have now been installed at the main chipmakers and can be tested for pilot production. Most importantly, the rapid improvement in EUV source power has restored credibility to the source roadmap and is a key enabler of the technology. Some important improvements remain to be demonstrated, but overall the technology is now getting closer to production.

Imec started work on EUV lithography in 2006, and from 2008 to 2011 was one of the 2 sites that had an EUV alpha-demo tool operational. Subsequently, Imec was one of the first 2 sites to install an ASML NXE:3100 EUV pre-production scanner, and in July of 2015 completed the installation of the ASML NXE:3300 EUV production scanner. In this presentation we will review the main progress that was made industry-wide over the last years, give current status of the EUV resists, masks, and scanner, and conclude with the main challenges that still lie ahead before EUV can become fully production worthy.

Biografie
Eric Hendrickx graduated from the University of Leuven in 1996, and subsequently from 1996 to 2001 was a postdoctoral research scientist at the University of Arizona (Optical Sciences Center) and the University of Leuven. In 2001 he joined the lithography department at imec, focusing on imaging and the characterization and on the introduction of the first 193nm high-NA immersion scanners into the imec cleanroom. In 2008, he started work on EUV lithography, and worked subsequently on ASML EUV Alpha-Demo tool, ASML NXE:3100 preproduction scanner, and ASML NXE:3300 scanner at imec. He currently is program manager at imec, and team lead of the imaging and reticles team.

Enabling low cost IoT ICs with lithography systems made in Europe

A. Mesquida Küsters
Sr. Director Product Marketing, Business Line DUV
ASML Netherlands B.V., Business Line DUV,
Veldhoven, Netherlands

Abstract
The internet of things (IoT) is the network of physical devices, vehicles, buildings and other items embedded with electronics, software, sensors, actuators, and network connectivity that enable these objects to collect and exchange data. In 2013 the Global Standards Initiative on Internet of Things (IoT-GSI) defined the IoT as "the infrastructure of the information society." The number of connected devices within the IoT semiconductor market was 17.7B in 2015 and is projected to be 74.8B in 2025, with a CAGR of 15.5%. This huge IC unit growth will not only drive silicon demand out of 300 mm- but also from 200 mm-factories, since a large variety of analog & power devices as well as sensors are produced in such factories. In these markets, European companies held a strong position and several of them are currently considering increasing the capacity of their 200 mm factories. One efficient way to achieve this goal is by exchanging older semiconductor manufacturing equipment by new state-of-the-art equipment able to deliver a 2 to 3 times higher silicon output per square foot of factory floor, as compared to tools built 15 to 20 years ago. During the presentation, we will explain using a comparative CapEx/OpEx-model for lithography equipment why the equipment retrofit approach could help to improve the competitiveness of European chip makers while minimizing CapEx investments.

Biografie
Antonio (Toni) Mesquida Küsters holds both Spanish and German nationalities and earned his master degree in Electrical Engineering (1990) as well as a PhD-degree in Semiconductor Science (1994) from the RWTH Aachen in Germany. Between 1995 and 2001, he held various management positions at Siemens AG (later Infineon Technologies AG) in Munich in the areas of IC development, technology transfer, product marketing and corporate venturing. As one of the founding members of Infineon Ventures, he served on the supervisory board of various high-tech start-ups around the world. Between 2002 in 2006, he held the position of Head of Corporate Strategy at the German MOCVD equipment provider AIXTRON SE. In 2006, he joined ASML in Veldhoven as Director of Market Intelligence, where he significantly contributed to the management directions and priorities of the Dutch company. Between 2011 and 2014, he served as Sourcing Director as well as Managing Director of the ASML German Operations in Alsdorf (former Xtreme Technologies), in the area of EUV DPP Sources. Since beginning of 2015, Toni is in charge of product marketing for all TWINSCAN dry lithography products.

Progress of Nanoimprint System Development for High Volume Manufacturing of Semiconductor Devices

H. Wada
Staff Engineer
Canon Inc., NGL Development Division 3, Tokyo, Japan

Abstract
Imprint lithography has been shown to be an effective technique for replication of nano-scale features. Jet and Flash Imprint Lithography* (J-FIL*) involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate.
Previous studies have demonstrated J-FIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. Additional considerations for inserting the technology into high volume manufacturing of semiconductor devices include overlay, throughput, defectivity, and mask infrastructure. Canon designs nanoimprint lithography tools by creating production infrastructure which includes resist production, collaborations with mask vendors, and close collaborations with the end user. This approach has resulted in the advancement of the technical requirements for high volume manufacturing mentioned above.
In this presentation, we will review the technology advancements made and introduce the new imprint systems that will be applied for the fabrication of advanced devices such as NAND Flash memory and DRAM. Cost of Ownership and future plans will also be discussed.

Biografie
Hideyuki Wada received his B.S. degree in physics from Osaka University in Japan, in 1990, and then started his career in semiconductor industry when he joined IBM Microelectronics Division where he was engaged in the semiconductor manufacturing process development as a photolithography engineer and process integration engineer. After 12 year experience with semiconductor device manufacturing, he entered a graduate school at the University of California at Los Angeles and then received his M.S. degree in electrical engineering in 2004. He had been working as a director of applications engineering to support customers for their nanoimprint technology developments in Japan and other countries in Asia, after he joined Molecular Imprints, Inc. in 2004. When the semiconductor business of Molecular imprints, Inc. was acquired by Canon Inc. in April 2014, he moved to newly established Canon Nanotechnologies, Inc., and then moved to Canon Inc.

Lithography efficiency: a cost comparison model

S. Grünzig
Principal Equipment Engineer Bump Engineering
GLOBALFOUNDRIES Dresden Module Two LLC &
Co. KG, BTF, Dresden, Germany

Abstract
The presentation shows a calculation model and conclusions with focus on the comparison of low-throughput and high-throughput lithography clusters via an analysis of the Cost of Ownership and applied data of the Overall Equipment Efficiency. Published documents up to today are not sufficient to prove that a higher throughput at a single lithography cell (consisting of linked Coater/Exposure/Developer) necessarily leads to an advantage of the manufacturing effectiveness. If the required conditions are given the calculated COO will show that it is efficient to operate with slower but with more cells.
The conditions will be shown as well as the metrics and the methodology to calculate the needed cell throughput and the corresponding count of lithography cells. The model enables to optimize the COO before the toolset will be bought. It will be possible because the COO and OEE are calculated the first time from the whole toolset point of view. This allows to add and to compare the influence of a new metric, the count of recipe changes. Known lithography throughput analyses excluded this naturally existing parameter in the past because the parameter is not visible if the throughput is calculated for a single lithography cell like usually done and propagated.
Furthermore, the calculation model presents a flexible method to identify not only the key drivers to run an efficient production but also easily to compare different scenarios. Two examples are shown, with models evaluated with real data.

Biografie
Sven Grünzig received his degree in Computer Science from the Dresden University of Technology in 1994. Past roles include Service Engineer/Product Specialist at Tokyo Electron and Lithography Consultant Equipment Engineering/Senior Staff Engineer at INFINEON/Qimonda. He supported Nemotek Technologie in Rabat as a Lithography Engineering Expert from 2010 and changed in 2012 to GLOBALFOUNDRIES Dresden. He now works as a Principal Equipment Engineer Bump Engineering.
Sven was a member of the team that was setting up the litho cell, printing the first 300mm wafer outside of a laboratory on December 18th, 1997 in the MOTOROLA/SIEMENS Pilotfab SC300. Thenceforth he focused on equipment reliability and productivity improvement. With an experience of more than 20 years by now in equipment analysis and optimization on both sides, equipment and chip maker, he acquired the expertise for an unique but plausible approach to analyze equipment conditions to enable an optimized set up, specifically for lithography cells and their production efficiency.

Rapid prototyping of nanodevices with the NanoFrazor

S. Weber
COO
SwissLitho AG, Zurich, Switzerland

Abstract
Thermal scanning probe lithography (t-SPL) [1] has recently entered the lithography market as alternative to electron beam lithography (EBL). By 2016, the first commercial t-SPL systems, called NanoFrazor®, have been installed at research facilities throughout Europe, America and Asia by SwissLitho - a spinoff company from ETH Zurich.

The technology has its origins at IBM Research and their Millipede project. At its core is a heatable probe tip which is used for creating and simultaneous inspection of nanostructures. The tip creates high-resolution (<10 nm half-pitch) features by local decomposition and evaporation of resist materials. The depth can be controlled for every pixel individually with about 1 nm accuracy, enabling arbitrary 3D nanopatterns in a single run. The speed of t-SPL is comparable to that of high-resolution Gaussian shaped EBL: 20 mm/s with a pixel rate of 500 kHz has been demonstrated [2]. The simultaneous inspection capability significantly improves accuracy and reliability and enables process turnaround times of mere seconds, because no resist development step is required. Furthermore, new stitching and overlay methods achieve sub-5 nm accuracy without the use of artificial markers.

Various pattern transfer methods like reactive ion etching, lift-off, electroplating, directed self-assembly have been demonstrated: Parallel lines with 18.5 nm half-pitch were etched 65 nm deep into Si, and various high resolution metal structures were fabricated using lift-off. The t-SPL process avoids high-energy, charged particles like electrons or ions which are known to damage or charge up certain materials while patterning which for delicate nanoelectronic devices can result in superior device performance. For example, top gates for InAs nanowire devices were made without trapped charge in the thin gate oxide under the electrodes.

[1] Pires, D. et al. Science 328, 732–735 (2010)
[2] Paul, P. C. et al. Nanotechnology 22, 275306 (2011)

Biografie
Stefan Weber studied at FU Berlin, where he received his Diploma and PhD in experimental physics. In 2007, he joined the EPFL/Institut de Microtechnique at Neuchâtel and the Group of Applied Physics (GAP) at the University of Geneva where he worked on Optical MEMS micromirror arrays. From 2011 to 2013 he was product manager and project leader for micro-optomechanical and optoelectronics modules for next generation lithography units at Jenoptik Optical Systems GmbH. Stefan joined SwissLitho AG in 2014 as COO, where he is responsible for all processes and operations.

Directed Self Assembly: Where are we? Where do we go?

I. Cayrefourcq
Director of Emerging Technologies
ARKEMA, Corporate R&D, Paris, France

Abstract
Directed Self Assembly (DSA) lithography has been a very hot topic these last years. Its use in various applications including contact repair, contact shrink and multiplication, line and space patterning, has been heavily studied and tremendous progresses have been made. After a few years of great (over?) excitement on DSA, we are now back to real world and work. While key achievements have been demonstrated in pattern fidelity (i.e. CDU, Placement error…) many challenges, such as defectivity, remain to be overcome before that DSA can become a viable patterning solution. In this presentation, after an overview on the DSA state of the art we will discuss the latest results and show that despite the remaining challenges, DSA is still a unique and promising technology that will complement classical lithography.

Biografie
Dr Ian Cayrefourcq is currently Director of Emerging Technologies at Arkema. He is leading both Renewable Energies and Electronics R&D portfolios. Before joining Arkema, he has been leading various organisation such as R&D departments, international project teams and New Business Development department in various high tech companies such as Thales, Corning and Soitec. Dr Ian Cayrefourcq owns an engineering degree in Material Science, A master Degree in Solid Physics and a PhD in microelectronics. He is author or Co-author of more than 70 publications and 20 patents in the semi-conductor field.