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TechARENA: Advanced Materials Session2

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imec

Biography
Johan Dekoster received the M.S. degree in Exact Sciences (Physics) in 1988 from the KU Leuven, Belgium. In 1993 he received the Ph.D. degree (Physics), also from the KU Leuven. From 1993 till 1999 he held postdoctoral fellowships from the Research Council and the Fund for Scientific Research at the Institute of Nuclear and Radiation Physics of the KU Leuven. In 1999 he joined the OTN business unit of Siemens. He was project leader for several development projects for data, voice, video and LAN. In 2007 he became program manager OTN at Nokia Siemens Networks. In April 2008 he joined imec as R&D manager of the Epitaxy group with responsibility on epitaxial deposition of group IV and III-V semiconductor materials. Since November 2012 he is program manager of the equipment and materials suppliers collaborations within the Semiconductor Technology and Systems unit at imec.

Ligands as Surfactants in CVD and ALD: Making and Modifying Metal Surfaces

S. Barry
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Carleton University, Chemistry, Ottawa, Canada

Carleton UNIVERSITY
Canada's Capital University

Abstract
Controlled deposition of metal films is important for many interesting applications, including microelectronics, as well as substrates for graphene fabrication, SERS and photochemistry. Deposition from the vapour phase offers superior control over purity and size of deposited metal structures, including films. However, shape control from the vapour phase remains a challenge.

Precursor compounds for chemical vapour deposition (CVD) and atomic layer deposition (ALD) can influence the shape of deposited metal structures and surfaces: computational studies show that a coordinative ligand can dissociate from the precursor and act as a surfactant,

controlling saturation of the surface and nucleation of metal-bearing moieties.
When applied in practice, a deposited metal surface can be controlled by judicious choice of surfactant: saturated N-heterocyclic carbenes are superior to phosphine when applied to a gold surface as surfactants, and produce smoother and more well-controlled crystalline surfaces. This concept can be extended to using free bases in the gas phase to limit surface growth and nucleation. Indeed, tetrahydrothiophene was used recently to form monolithic, single gold features with up to 20 square micron (111) plateaus.

The design and choice of coordination ligands in metal-containing precursor compounds will be discussed, with emphasis on their role as a surface-controlling surfactant. Examples of CVD and ALD deposited films will be given, and computational modeling of surface chemistry will be presented.

Biografie
Seán Barry is a Full Professor at Carleton University, Ottawa, Canada), where he works on precursor compounds for atomic layer deposition (ALD).

Seán was trained in inorganic synthetic chemistry by Darrin Richeson (PhD, University of Ottawa, 1996), and spent three years working on chemical vapour deposition (CVD) and ALD precursors in the group of Roy Gordon (PDF, Harvard University, 1998 – 2000, 2002 -2003). He was instrumental in the design and synthesis of the well-known copper amidinate dimers that are presently used for copper CVD/ALD.

He started in Carleton University in 2003 working on guanidinates of the group 13 metals (Al, Ga, In), and has recently studied guanidinates, iminopyrrolidinates and carbenes of the coinage metals (Cu, Ag, Au) for depositing thin films of these metals. His group works mainly on the mechanisms of thermal decomposition and thin film deposition, and have invented several novel characterization methods to better understand mechanism.

He was previously the founder and Senior Scientific Advisor for Precision Molecular Design, a start-up company with GreenCentre Canada to commercialize precursors for atomic layer deposition. Seán is also the director of the Facility for Nanoscience, Surfaces, and Sensor Interfaces (FANSSI), which was commissioned in 2015 by a $1.9M Canadian infrastructure grant to study surface chemistry and ALD.

He is recognized as a world expert in metal ALD and precursor design. He has long-standing and extensive industrial collaborations in ALD, including Applied Materials, Air Liquide, the Royal Canadian Mint, and BASF, to name a few. He has over 50 papers and 6 patents and patent applications in ALD precursor and process design:4 of the patents were established while an independent researcher at Carleton.

In 2012, he was awarded a Marie Curie Fellowship as part of the EU-funded European Research Training Network ENHANCE to undertake metal ALD at the University of Helsinki, and in 2015 he was awarded a $295k Vinnova VINNMER Mobility grant to undertake CVD/ALD research in Sweden.

New materials for More Moore and More than Moore

F. Martin
Senior Scientist
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Grenoble, France

Abstract
New processes and materials are emerging to provide possible solutions at the crossroad of MOS scaling and diversification of devices for More than Moore and IOT, including sensors, memories, power devices, RF and optoelectronic devices... New materials like 2D dichalcogenides could provide solutions but promises can become reality if manageable processes can be implemented on large substrates. This talk will discuss our motivation to investigate “green” processes avoiding toxic or corrosive precursors and the solutions brought by organometallic chemistries to promote new ALD or MLD deposition processes. Results on Molecular Doping for semiconductor surface doping and MoS2 (WS2) synthesis by Molecular Layer Deposition will be presented and discussed in a more general frame, aiming to promote manageable solutions for smart materials and interfaces tuning towards sustainable and low cost IOT devices.

Biografie
François Martin, 59 years old, is senior scientist in the Thin Film Deposition team in LETI. He was involved in the past decades on Material research and Developments for Advanced CMOS and memories, including HighK/Metal gate stacks for advanced CMOS. He brought his contribution to the introduction of Atomic Layer Deposition for HighK deposition in LETI and participated to European projects on advanced FEOL developments. His field of interest for several years is the research in emerging materials and processes like Molecular Layer Doping and 2D Dichalcogenide deposition in relationship with academic skills dealing with organometallic chemistry, aiming for sustainable processes and materials availability in future nanoelectronic devices. He was also member of the Emerging Material Section of the ITRS (2006-2014).

2D materials and heterostructures: Fabrication Technology and processes

R. Sundaram
Market Manager : Research and Emerging Technologies
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Abstract
Two dimensional materials are gaining a lot of interest as a possible strategy for pushing the scaling limits as well as for heterogeneous integration in micro/nano electronics. Fabrication of 2D materials and electronic devices require tailored solutions for the deposition and etch of these atomically thin materials. In this talk, I will present the technology and processes developed at Oxford Instruments for the atomic scale processing and quality control of 2D materials. This will include equipment and processing for deposition and etching of 2D materials by CVD, ALD and ALE as well as deposition of high k dielectrics on such materials for optimum device performance. In addition, the possibility of creating novel functional architectures by in situ deposition of 2D heterostructures will also be outlined.

Biografie
Dr Ravi Sundaram is the Market manger for emerging technologies at Oxford Instruments Plasma Technology. He has been involved in 2D materials research in several institutions such as EPFL, Switzerland, Max Planck Institute Stuttgart, Germany, IBM T.J Watson Research Labs, NY and Cambridge University where he worked on several aspects of graphene and 2D materials from synthesis, fundamental science to prototype applications in optoelectronics and electronics. He joined Oxford Instruments to lead and coordinate efforts towards 2D materials R&D and is now responsible for scoping out and developing a strategy for emerging technology markets.

From Bulk Gallium Nitride Material to Vertical GaN Devices

T. Mikolajick
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Scientific Director of NaMlab gGmbH
Namlab and TU Dresden, Dresden, Germany

Abstract
Due to its direct and large bandgap Gallium Nitride is an essential material for optoelectronics and holds many promises for power semiconductor devices. In the last few years several new devices based on GaN epitaxial grown on large silicon wafers with voltage classes up to 600V have appeared on the market. However, to unfold the full potential of the technology, a vertical device architecture would be highly desirable. This will require bulk Gallium Nitride wafers rather than producing the Gallium Nitride on a foreign substrate like Silicon, Silicon Carbide or Sapphire. The most promising route to an economic production of bulk Gallium Nitride substrate is Hydride Vapour Phase Epitaxy (HVPE) growth. In the first part of this talk, the HVPE growth will be described together with recent results on wafer doping during growth. In the second part a pseudo vertical MOSFET technology on Gallium Nitride substrates will be presented together with first device results. Bringing both aspects together can be the basis for a high performance power semiconductor Gallium Nitride technology of the future.

Biografie
Thomas Mikolajick received the Diploma (Dipl.-Ing.) in electrical engineering in 1990 and his phD in electrical engineering in 1996 both from the University Erlangen-Nuremberg. From 1996 till 2006 he was in the semiconductor industry developing CMOS processes, Ferroelectric Memories, emerging Non-volatile Memories and Flash Memories first at Siemens Semiconductor and later at Infineon. In late 2006 he moved back to academia taking over a professorship for material science of electron devices and sensors at the University of Technology Freiberg, and in October 2009 he started at Technische Universität Dresden were he now holds a professorship for Nanoelectronic Materials in combination with the position of scientific director at NaMLab GmbH. Since April 2010 he is the coordinator of the “Cool Silicon” Cluster in Dresden. Prof. Mikolajick is author or co-author of more than 300 publications in scientific journals or at scientific conferences and inventor or co-inventor of about 50 patents

Towards Graphene-based heterojunction devices for microelectronic applications

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Abstract
The integration of dielectrics or semiconductors on Graphene is of critical importance for the development of a new generation of Graphene-based hetero-junction devices. The deposition of a high-k dielectric, like Al2O3 or HfO2 or of Silicon on top of Graphene is still challenging due to Graphene's lack of dangling bonds. In this paper, two strategies for the dielectric-Graphene and Silicon-Graphene integration will be presented.
Atomic Layer Deposition (ALD) or Atomic Vapour Deposition (AVD) processes have been explored to deposit high-κ dielectrics on Graphene with negligible damage of the Graphene layer. However, the nucleation of the dielectric film is hindered by the chemical inertness of the Graphene surface. Therefore, the initial ALD or AVD growth on Graphene requires a functionalization of the pristine Graphene surface with reactive groups.
Plasma enhanced CVD (PECVD) is of interest for applications requiring low thermal budgets such as the back end of line (BEOL). However, high energy ion bombardment related to plasma exposure readily correlates with worsening of material properties. We demonstrate, that by the use of PECVD at a very high frequency of 140 MHz, thin a-Si:H layers can be grown softly without changing the properties of the underlying Graphene significantly.
The herein presented deposition strategies for dielectrics and semiconductors on Graphene surfaces demonstrate a significant progress towards a complete fabrication scheme of Graphene-based heterojunction devices in microelectronic technologies.

Biografie
Christian Wenger received the Diploma in physics from the University of Konstanz, in 1995 and the Ph.D. degree from the Technical University of Dresden, in 2000. Since 2002, he has been with the Innovations for High Performance Microelectronics (IHP), where he works in the field of functional devices for medical and space applications. In 2009, he received the post-doctoral degree at TU Dresden. He has authored and co-authored more than 150 papers and holds 6 patents.

Gate-All-Around MOSFETs based on Vertically Stacked Horizontal Nanowires

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Abstract
Gate-all-around (GAA) transistors based on vertically stacked horizontal nanowires are promising candidates to replace FinFETs in future CMOS technology nodes. First of all, GAA devices provide optimal electrostatic control over semiconducting nanowire channels, which enables downscaling of the gate length to below the FinFET limit, while maintaining low off-state leakage [1]. Besides, horizontally oriented nanowires are an evolutionary extension of FinFETs, as opposed to vertical nanowires which require more disruptive technology and design changes [2]. Finally, stacking of nanowires is relevant for enhancing the drive current per footprint. Based on these considerations, GAA transistors made of vertically stacked horizontal nanowires have been included in the ITRS roadmap to reduce the contacted gate pitch, which is a key figure of merit for CMOS device density, to below ~40 nm in 2019-2021 [3].

In the context of the industrial relevance described above, we present the fabrication of Si GAA devices on bulk Si substrates. Multiple processing aspects that are relevant for bulk CMOS technology definition are addressed, including stacking of 8-nm-diameter Si wires at 45-nm lateral pitch and 20-nm vertical pitch [4], and nanowire-compatible replacement metal gate processing in combination with threshold voltage tuning by dual work function metal integration [5]. Temperature restrictions for the formation of shallow trench isolation, and the interaction between N- and P-type junction formation on one hand and nanowire release processes on the other hand are discussed as well.

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[2] L. Liebmann et al., VLSI Tech. Dig., p.112 (2016).
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[4] H. Mertens et al., VLSI Tech. Dig., p.158 (2016).
[5] H. Mertens et al., IEDM Tech. Dig., p.524 (2016).

Biografie
Hans Mertens is a principal member of technical staff at the international nanoelectronics research center Imec, based in Leuven Belgium. His main research interest is gate-all-around process integration based on group-IV semiconductors. Prior to joining Imec in 2012, he was a senior scientist at NXP Semiconductors, working on SiGe BiCMOS technologies for RF small-signal applications. Hans Mertens holds a M.Sc. degree in Applied Physics from Eindhoven University of Technology, and a Ph.D. degree in Physics from Utrecht University, both in The Netherlands.