450mm

L. Pfitzner
Vice President for External Strategic Affairs
Fraunhofer IISB, Erlangen, Germany

Biography
Lothar Pfitzner holds an M.S. (Dipl.-Ing.) degree in material science and Ph.D. (Dr.-Ing.) in electronics engineering, both from the University of Erlangen-Nuremberg. From 1976 to 1985 he worked as a lecturer at the Engineering Faculty at the University of Erlangen-Nuremberg. Since 1985 he was heading the department 'Semiconductor Manufacturing' of the Fraunhofer Institute of Integrated Systems and Device Technology (IISB) in Erlangen, performing research and development in the fields of processing technologies and equipment developments in Front-end-of-line and Back-end-of-line, and manufacturing optimization with some focus on advanced process control, metrology, integrated vacuum cluster tools and contamination control. 'In 2003, he was appointed "Professor for Micro-/Nanoelectronics. Since 2014, he is appointed Vice President for External Strategic Affairs of the Fraunhofer IISB.

Continued Progress on 450mm Development

F. Robertson
VP/GM
G450C, Albany, NY, United States

Abstract
The Global 450mm Consortium (G450C), a public/private program based at the College of Nanoscale Science and Engineering (CNSE) in Albany, NY, is preparing for the 450mm transition with a broad set of enabling and collaborative efforts spanning the semiconductor industry worldwide. Good progress continues in the core program with comprehensive test wafer process and metrology capability available on excellent quality (SEMI M1!) silicon wafers, a significant tool set already installed at the CNSE cleanroom or available at Supplier sites and many further additions this year and next.

As part of enabling tools for demonstration, G450C member company assignees and Supplier technical staff are working together to move the current capability to more advanced technology and readiness for High Volume Manufacturing. G450C updated its Equipment Performance Metrics to Sub-10nm this year with broad industry input and is currently working on the first demonstrations using globally-aligned standard methods. These demos include two tools being coordinated between G450C and the ENIAC SEA4KET program (one in Albany and one in Leuven).

A key element of the program strategy over the 450mm development period is to identify and demonstrate

elements beyond developing and demonstrating tools that might improve productivity, address technology needs or enhance industry sustainability regardless of wafer size. The intersection of EHS objectives, efficient facilities systems and control of wafer ambient conditions for future technology needs has been rich ground for multiple collaborations between G450C, the Facilities 450mm Consortium (F450C), SEMI members and EEMI450/Metro450 participants.

Our presentation will provide an update on progress in the tool set, wafer quality, test wafer support capability and the global collaborative efforts to address key topics with benefit beyond 450mm.

CV of presenting author
Frank Robertson is Vice President and General Manager for Industry Interface and Program Strategy at the Global 450mm Consortium (G450C) based at the College of Nanoscale Science and Engineering in Albany, New York. His objective is to drive a cost-effective transition to the larger wafer size by ensuring support capabilities are available to enable Supplier development and by pursuing pre-competitive collaboration opportunities with Suppliers and other organizations.

Before being assigned by Intel to G450C Frank managed External Programs for its Technology and Manufacturing Group, helping consortia, universities and government agencies keep the R&D pipeline filled with promising new work.

Prior to joining Intel in 2000 Frank was Vice President and Chief Operating Officer of SEMATECH. In that role, he led the technology development programs and the consortium's transformation into an international organization.

Frank was Vice President and General Manager of the International 300mm Initiative from 1995-1998. This global cooperative effort resulted in major industry cost savings through standardization and by leading equipment development for that wafer size transition.

He spent a couple of decades before that in wafer fabs and started a company developing optical storage media to make use of his chemistry degree.

Eco system requirements to enable further system scaling and semiconductor manufacturing effectiveness

L. Lauwers
Vice President Business Development
Imec, Leuven, Belgium

Abstract
In the foreseeable future, we can rest assured that new application platforms will continue to drive the IC industry: Internet of Things, personal health management, ever increasing connectivity...
Moore's Law has made the applications of today possible through a continuous cost reduction of transistors, enabling more complexity, functionality and performance of systems.
Which materials, device and process technologies will we be able to bring to a manufacturable level in order to keep that pace, and to allow for next generation process platforms to offer benefits to the designers?
Which measures are required in the ecosystem: material research and equipment R&D, in order to bear the continuously increasing cost of R&D in a climate of growing consolidation?
It's a matter of scale and volume: will we have products which will generate sufficient volume in a sustainable way to enable further ecosystem development, amongst which the 450 wafer size developments, or other capital intensive transitions?
Our imagination will lead the way.

CV of presenting author

Lode Lauwers is Vice President Business Development in IMEC, the nanoelectronics R&D Center in Leuven, Belgium.
He oversees Corporate Business Development of IMEC Business Lines, CMOS scaling, Smart Systems and Energy, with a shared responsibility over sales with VP world wide Account Management. In the area of CMOS technology, he is responsible for IMEC business offerings, covering collaborations with leading IC manufacturers and equipment and material suppliers worldwide.
Since he joined IMEC in 2005, he had various roles in IMEC's technology business and sales, a.o. as Director Strategic Program Partnerships, and having Regional Sales responsibility for IMEC business in Japan.
Earlier, he has been general manager of an ASIC design house, part of a US-based ASSP provider for the telecom industry, and scientific advisor for government funding in local and European cooperative networks in micro-electronics and telecommunications.

Sustainability challenges in the 450mm technology node

A. Maynes
F450C Program Manager
Facilities 450mm Consortium (F450C), Albany, United States

Abstract
The industry continues to make positive strides with the transition to the next generation 450mm wafer size. Experts in semiconductor development are striving to make 450mm a reality from a technical and manufacturing standpoint. Along with the increase in wafer size, the industry is closely examining impacts to the facility infrastructure, as merely scaling the manufacturing process is not a practical option. The size of the 450mm facility infrastructure and its associated utility consumption projections would simply exceed affordability and resource availability.

The facility specialists involved in establishing and later implementing 450mm infrastructure requirements are facing the same degree of challenges as the IC and equipment manufacturers. Global 450 and Facility 450 Consortia leaders are collaborating closely with five of the industry's top IC manufacturers to bring their collective expertise to bear on the most pressing 450mm fab issues. They are also looking to apply lessons learned from 450mm development to existing 300mm wafer fabs. The consortia focus specifically on safety, cost, schedule, sustainability, and environmental footprint, with a goal of reducing the cost of production, increasing productivity for manufacturers, and improving the efficiency of utility consumption.

This presentation will address these various infrastructure requirements and challenges for a more sustainable manufacturing process, including recommendations to optimize 300mm manufacturing. The session will be presented by Adrian Maynes, Program Manager of the Facilities 450mm Consortium (F450C).

CV of presenting author
Adrian Maynes was appointed as the M+W U.S., Inc. Program Manager for the Facility 450mm Consortium (F450C) in August of 2013. The Facilities 450mm Consortium (F450C) is a first-of-its-kind partnership at SUNY's College of Nanoscale Science and Engineering (CNSE) that is leading the global effort to design and build next-generation 450mm computer chip fabrication facilities. The collaboration includes 10 of the world's leading nano-electronics facility companies. Members of the F450C are working closely with the Global 450mm Consortium (G450C - Intel, GLOBALFOUNDRIES, IBM, TSMC, Samsung), to identify viable solutions required for 450mm high-volume facility construction, with initial focus areas to include reducing tool installation cost and duration, and improving facility sustainability.

Prior to his appointment as Program Manager, Adrian ventured into the heart of Latin America's emerging economy to assemble a business strategy & market growth plan for Mexico. Centrally located to Mexico's business climate in the Federal District of Mexico City, the M+W Mexico Platform was formally established

on October 12, 2011.
Adrian worked closely with Executive Management to build a lean & local team while retrofitting & furnishing a start-of-the-art 8,000 square foot country headquarters. The Mexico Platform has exceeded $100M USD in sales, and currently employs 30 Mexican nationals.

When M+W U.S., Inc. had their sights set on the growing photovoltaic industry in 2008, Adrian directed Business Development efforts to establish market presence. While cultivating business prospects with a skilled team of architects, engineers, and executive management, Adrian's team helped generate $155M in revenue.
Upon joining M+W U.S., Inc. in 2006, Adrian served as the Platform Lead for Industrial Engineering, where he worked to engineer facility requirements for much of SUNY's initial semiconductor research & development space. He also helped create preliminary design for AMD's Fab4X - an effort that eventually morphed into the Global Foundries project in upstate NY.

Scaling Options in Relation to 450mm

M. Liehr
Executive VP for Innovation & Technology
CNSE, Albany, United States

Abstract
The nanoelectronics industry has enjoyed decades of productivity gains driven by lithographic scaling. However, scaling slowed due to delays in the introduction of extreme ultraviolet (EUV). New materials were introduced which help to drive increases in performance or reductions in power consumption. However, to maintain the pace of die-level cost reduction, a different set of approaches have been proposed, only one of which is to use EUV. Two other approaches are being pursued, a transition in wafer size to 450mm and chip stacking. All three face the challenge of becoming cost-effective prior to wide-spread adoption. Lastly, the equipment industry is challenged to develop novel materials solutions as required for device scaling in parallel for 300mm and 450mm.

The first generation of EUV production scanners are currently being delivered. One such scanner is being installed at CNSE with the goal of start of development activities in 2Q2014. The scanner will be for development of sub-10nm technology node CMOS, as well as to support advanced resist and mask development. Initial 193nm based directed self-assembly work in support of G450C has led to additional development work on 300mm in CNSE.

Chip stacking technologies, either via interposers ("2.5D") or chip stacks ("3D"), are being developed by a wide range of R&D organizations and companies world-wide. No standard integration scheme has emerged yet due to constraints in yield management or limitations in equipment cost of ownership. However, this technology aims at current wafer sizes of 300mm, with a migration to 450mm gated primarily by the general pace of the 450mm transition.

The timely availability of novel materials in conjunction with a manufacturable process is critical for continued scaling. The recent re-assessment by G450C of the likely CMOS node for the wafer transition opens up a new set of process options to evaluate, based on the industry introduction of materials needed for sub-10nm CMOS.

CV of presenting author
As CNSE Executive Vice President of Innovation and Technology, Michael Liehr focuses on the creation of new business opportunities and manages integrated industry-university consortia and public-private partnerships. He is also responsible for the effective and efficient operation of the CNSE core strategic semiconductor and packaging partnership engagements, including the IBM, GLOBALFOUNDRIES, SEMATECH, AMAT, TEL, and LAM partnerships.

Prior to this assignment, he led the Global 450mm Consortium through the start-up phase as the General

Manager. Dr. Liehr is further the Vice President for Research at the College of Nanoscale Science and Engineering in Albany, NY. Prior to joining CNSE, Dr. Liehr served as an IBM executive responsible for Worldwide Semiconductor Manufacturing Strategic Production Alliances for leading-edge semiconductor products.

450mm synergies for smaller wafer diameters: contamination control

O. Kievit
Projectmanager
TNO, Industrial Innovation, Delft, Netherlands

Abstract
Uncertainties about the introduction of 450mm wafers in high volume manufacturing are increasing and delay is expected. As a consequence, questions arise on how R&D activities targeted at 450mm technology can be re-directed towards smaller wafer sizes and other areas of semiconductor manufacturing. A successful transfer of 450mm innovations to other areas is important to ensure the continuity and profitability of the semiconductor industry.

In this presentation we will give a view on 450mm synergies from the perspective of the Research Institute TNO. We will show that contamination control developments for the 450mm platform can also be applied to 300mm and Xnm equipment and processes. In addition to current and planned research activities on molecular and particle contamination control, the presentation will include strategies and opportunities for applications beyond the 450mm transition.

CV of presenting author
Dr.ir. Olaf Kievit is Project manager in the Industrial Innovation department at TNO. He graduated in 1990 for his MsC in Chemical Engineering and obtained a PhD in Aerosol Technology at Delft University of Technology in 1995. Olaf worked at 3M Corporation for 6 years, developing new technology for air filtration. He joined TNO in 2001 as a project manager and research scientist. Focusing more and more on project management, he has been active in the field of high end equipment development for over 10 years. Olaf was and is involved in the definition and execution of several European projects including EEMI450, EEM450PR, E450EDL, SEA4KET and E450LMDAP. He currently manages a number of international research projects.

B. Capraro
EU Research Programme Manager
Intel Ireland Ltd, F24 Research, Leixlip, Ireland

Biography
Bernie Capraro - Intel Ireland EU Research Programme and Project Manager
Bernie received a Masters Degree in Engineering(MEng)with Distinction from Newcastle upon Tyne Polytechnic and has been working at Intel for the past 17 years holding various Engineering and Management roles across all four wafer fabrication facilities. Bernie is currently responsible for all silicon nanotechnology EU projects involving Intel Ireland, delivering potential solutions for materials, equipment and processing techniques required for the future technology nodes. Bernie's semiconductor career spans 27 years, with other Process and Equipment Engineering positions held at Telefunken GmbH, Nortel/Bell Northern Research, Applied Materials and Newport Wafer Fab.

450mm specifications will boost the 300mm yield in wafer manufacturing

D. Rousset
Office Director
CATRENE, PARIS, France

Abstract
The 450 mm wafer transition has been initiated since 2009 with the first attempt to propose a new wafer size.

EEMI450 project has been launched by the European Equipment and Materials Industry in order to stimulate activities on 450mm. The semiconductor total demand has recorded a CAGR of 7.6%, extrapolating this growth rate, the amount of silicon shipped would double in just less than 10 years.

The challenge for chip maker choosing to adopt 450mm will be to get yielding die similar than 300m. The yield hunting became the main worry. Defect inspection and metrology steps absent or subsidiary in the 300mm wafer manufacturing have been introduced for 450mm.

CATRENE and ENIAC has facilitated the creation of projects to deliver solution for preventing all kind of contamination. Process equipment manufacturers develop tools that reduce contamination in the FOUP and are developing cleaning process free from added particles. Wafer manufacturers develop extremely flat wafer substrates with high uniformity roughness.

The G450C initiative has allowed the definition of the EPM (Equipment Performance Metrics). This worldwide cooperation has been supported by the emergence of many SEMI specifications solidifying the quality standard of the 450 mm equipment.

During the last months a question is circulating : can we adopt the 450mm specifications to the 300mm wafer manufacturing ?

The increased 300mm volume will require a steady improvement of the yield. This means smaller process windows and constant reduction of defect density. Obviously the processes will also require continuous monitoring to identify and reduce the cause of process variation.

The retrofit of the 450mm specifications to the 300mm equipment will provide a boost to 300mm wafer manufacturing yield and a direct return of the R&D effort spent of the 450mm. In the perspective of cost reduction of the 300 mm, it is mandatory for the actors to keep running initiatives in the 450mm ecosystem to be ahead.

CV of presenting author
Denis has the Director for Programme Technologies at CATRENE (Cluster for Application and Technologies Research in Europe on Nano-Electronics) since July 2012and now he is CATRENE Office Director on top. He is still monitoring a hand full of collaborative projects focusing on Advanced CMOS process, Equipment, New Materials and Manufacturing. Just before, Denis leaded the Public Affairs department at ST-Ericsson, world leader in development of wireless platforms and semiconductors, thus defining and managing worldwide collaborative programs during 4 years. He started his career at Motorola in Toulouse, France, in process engineering, before moving to STMicroelectronics (formerly Thomson Semiconductors) in 1983. From a telecom product engineering manager, he became the telecom marketing manager in charge of North America. Back in Europe in 2001, he became key account manager for Alcatel Mobile Phones and was thus directly involved in the integration of the Alcatel teams following the acquisition of Alcatel's mobile telephone business. In 2002 he also participated in the organization of the first GSM Platform at STMicroelectronics. In 2005, Denis took the responsibility of the key account management for Ericsson's Mobile Platform until the creation of ST-Ericsson, the joint-venture of STMicroelectronics wireless business and Ericsson Mobile Platforms in 2009. Denis holds a Bachelor of Engineering from the Ecole Nationale Supérieure de Radioélectricité of Bordeaux (France) and participated in an executive training program at the Harvard Business School.

Semiconductor Equipment Assessment for Key Enabling Technologies (SEA4KET)

M. Pfeffer
Group Manager
Fraunhofer IISB, Manufactuirng Control, Erlangen, Germany

Abstract
This talk gives an update on Semiconductor Equipment Assessment activities within the EU funded project SEA4KET. SEA4KET is the continuation of the European success story SEA, which began 1996 and lasted until 2004. In 2006, Fraunhofer IISB took over the role to drive Semiconductor Equipment Assessment forward by setting up several European Integrated Projects (IPs) taking the consequent step from equipment R&D to equipment assessment qualification. The recent one, SEA4KET concentrates on process and metrology systems for important enablers of future technologies: 450 mm wafer equipment but also SiC material and 3D processing. The talk will also report on AMC and contamination control activities as one specific part for 450 mm equipment assessment and will comment the refocusing on 300 mm aspects.

CV of presenting author
Dr. Markus Pfeffer- Group Manager Fraunhofer IISB

Dr. Markus Pfeffer holds a diploma in Electrical Engineering and a PhD (Dr.-Ing.) with specialization in manufacturing optimization both from the University of Erlangen- Nuremberg. Since 2002 he is with Fraunhofer IISB in the department Semiconductor Manufacturing Equipment and Methods. He leads the group Manufacturing Control and is responsible for the analysis laboratory for micro and nano technology at the IISB.
He has been engaged in the fields of equipment control, advanced process control, manufacturing optimization, analytical methods, equipment assessment and especially discrete event simulation. He was/is involved in several national and international cooperative R&D projects, e. g. FLYING WAFER, IMPROVE, EEMI450, EEM450PR, SEA-NET, SEAL and SEA4KET in different functions also as coordinator. He is member of the Steering Committee of the 450mm Equipment & Materials Initiative EEMI450 and since 2012 a member of the Factory Integration Group and Yield Enhancement Group of the ITRS.

M. Pfeffer
Group Manager
Fraunhofer IISB, Manufactuirng Control, Erlangen, Germany

CV of presenting author
Dr. Markus Pfeffer- Group Manager Fraunhofer IISB

Dr. Markus Pfeffer holds a diploma in Electrical Engineering and a PhD (Dr.-Ing.) with specialization in manufacturing optimization both from the University of Erlangen- Nuremberg. Since 2002 he is with Fraunhofer IISB in the department Semiconductor Manufacturing Equipment and Methods. He leads the group Manufacturing Control and is responsible for the analysis laboratory for micro and nano technology at the IISB.
He has been engaged in the fields of equipment control, advanced process control, manufacturing optimization, analytical methods, equipment assessment and especially discrete event simulation. He was/is involved in several national and international cooperative R&D projects, e. g. FLYING WAFER, IMPROVE, EEMI450, EEM450PR, SEA-NET, SEAL and SEA4KET in different functions also as coordinator. He is member of the Steering Committee of the 450mm Equipment & Materials Initiative EEMI450 and since 2012 a member of the Factory Integration Group and Yield Enhancement Group of the ITRS.

The dawn of 450mm production: Batch and single wafer equipment and process exploration

C. Herbschleb
Process Engineer
ASM Europe BV, R&D, Almere, Netherlands

Abstract
C.T. Herbschleb, T.G.M. Oosterlaken, R. De Blank, S. Strausser, J. Cossins, M. Boy (Siltronic)

ASM was involved in the 450 mm transition from an early stage, and has designed and developed 450 mm pilot systems. Currently, two systems are installed in the Global 450 mm consortium clean room in Albany, New York. The first system is a single reactor batch furnace, capable of dry and wet oxidation processes, hydrogen cures, and in situ DCE cleans up to temperatures of 1000 C. Its load size is 100 product wafers; it comprises one load port and intermediate wafer storages. An exchange track dominates the appearance of the backside of tool, which facilitates easy maintenance, as tool components have increased in size and weight. The general hardware of the furnace will be described, as well as data on uniformity for thin dry oxides and thick wet oxides. In addition, designs used and tested in the 450 mm tool which can be back-integrated into 300 mm equipment of ASM will be covered, and their benefits for logistics, serviceability, and thermal performance will be explained. The second ASM 450 mm system at G450C to be described is a processing tool having four dual chamber modules capable of PECVD and PEALD applications. This system has been in operation since mid-2012, and an overview of the performance data achieved to date will be given, as well as a general description of the tool and some of its key features for 450 mm.

CV of presenting author
Cornelis (Kees) Herbschleb graduated from Leiden University in 2006 and obtained a PhD at the same university in the interface physics group. In 2011 he joined ASM as a process engineer, specifically for process development on the 450 mm equipment; currently he is the lead technical engineer on the 450 mm tool, concerting activities on this equipment of partners within European 450 mm projects including EEMI450 and SEA4KET.

AMC contamination management strategy for 450mm

M. Davenet
R&D Collaboration and Funding Manager
adixen Vacuum Products, annecy, France

Abstract
Airborne Molecular Contamination (in short AMC) was demonstrated to be critical for yield, especially and quality in the semiconductor manufacturing. Sub ppb levels of contamination such as acids or HF can strongly degrade process performance and decrease product yield. Fab airbone molecular contamination should be managed, as stated by ITRS guidelines, especially for next generation devices with small dimensions and large wafer substrates (450 mm)
In this article, we propose to propose and discuss AMC contamination management strategy for 450mm fab. We will review and discuss the various R&D projects launched on AMC contamination management. Especially, roadmap and development status for 450mm AMC advanced solutions as well as European R&D activities on AMC in the context of 450mm challenges will be reviewed and discussed.
Finally, we will conclude with a review and discussion on a proposed strategy for AMC contamination

management for coming challenges.

CV of presenting author
adixen Vacuum Products is leader in AMC solutions since 2008 and participates to numerous European collaborative R&D projects, including next generation 450mm project.
Magali Davenet (Graduate in Optical Engineering school in 2000 and graduate in Executive International MBA in 2014) is responsible for collaboration and funding at adixen.She is involved in various microelectronic projects, including advanced 450mm projects.

Upsizing Wafer Fab UPW Needs to 450mm Demands

H. Mueller
Microelectronics Manager
Georg Fischer Piping Systems, GMDI BKS3918, Schaffhausen, Switzerland

Abstract
The long awaited upsizing of wafer fab utilities to accommodate 450mm wafer production has begun. Fabs are either built, under construction, in modification or planned on future roadmaps. Major stakeholders such as Intel, GLOBALFOUNDRIES, Samsung and TSMC continue to push equipment suppliers to these inevitable larger wafers.

Outfitting a new fab (Greenfield) or providing a future expansion (Brownfield) with the various assortment of UPW piping systems needed to make all the twists and turns from the Central Utility Building to the wet bench offers polymer component suppliers a unique challenge.

The authors wish to present a segmented approach for 450mm piping designs that can get the end-user/installer from the largest pipe necessary to tool hook-up and put some light on the completely controlled manufacturing processes required to meet the increasing specification demands for UPW used in the next generation Fabs.

CV of presenting author
Working in the Microelectronics Industry since 1994 in various functions:
PRESENT PROFESSION
Microelectronics Segment Management Georg Fischer Piping Systems Ltd. Schaffhausen, CH
EDUCATION
University Karlsruhe (TH) Karlsruhe, Germany
Mechanical Engineering Degree: Dipl.-Ing. Mechanical Engineering
RELATED EXPERIENCE
2004-Present: Market Manager Microelectronics
Outstanding achievements:
- Sustain product development for 450mm PVDF High Purity Piping System and introduction to the market:
2002-2004: SCP Germany Pliezhausen, GE
Engineering Manager Automated Wet Processing Tools
1998-2002: CFM/Mattson Technology Pliezhausen, GE
Manager Mechanical Engineering AWP
Outstanding achievements:
1994-1998: STEAG MicroTech Pliezhausen, GE
Designer/Team Leader Mechanical Engineering

Innovative Semiconductor Solutions supplied out of Silicon Saxony

J. Kinauer
Director Business Development/ Sales Semiconductor
AIS Automation Dresden GmbH, Dresden, Germany

Abstract
Saxony has developed itself to the largest semiconductor area in Europe, based on its versatile ecosystem of research, universities, suppliers and manufacturing. As a fact, the 1st 1 MB Chip in Eastern Europe was manufactured in Dresden in 1989 and the 1st 300mm Testline was installed in Dresden in 2000.

One reason for this success are the agile activities within Silicon Saxoy Cluster. To continue this success story, Silicon Saxony has started the working group SET-UP 4 FIFTY (Saxon Equipment Team - Update for Future Innovation Fab Technology) in the year 2013, This cluster of institutes and companies out of Saxony, are working together on next generation semicondcutor technologies and solutions.

This presentation will supply an overview of the companies and activites of the Silicon Saxony SET-UP 4 FIFTY Cluster and the competencies that are bundled in the Silicon Saxony Area. Examples of european funded projects for technology, automation and equipments, supplied by companies out of Saxony will demonstrate the innovationpool of our cluster members.

CV of presenting author
Jochen Kinauer:

Jochen Kinauer is Director for Sales and Business Development at AIS Automation Dresden GmbH, a company within the Meyer Burger Group with its headquarter in Dresden, Germany and operations around the globe. AIS Automation specialises in equipment automation as well as MES installation and has more than 80 MES installations and automation projects worldwide.
Jochen Kinauer previously worked as project manager for several hardware and software automation projects in the PV & semiconductor industry and is Leader of the Silicon Saxony 450mm and RFID Cluster. He holds a degree in Electrical Engineering, Controls & Automation from the Technical University of Munich.

B. van Nooten
Founder
Semi Consulting, Bilthoven, Netherlands

Biography
Sebastiaan (Bas) van Nooten graduated with a Master's degree from the Technical University Delft in 1971. After his military service he was involved in processing and design of integrated circuits till 1981 at Telefunken, Germany. After his return to Holland he went to an IC design house as group leader. In 1985 he moved to the semiconductor equipment industry in several positions, mainly as European product specialist for several equipment types. He joined ASM in 1989, first heading the German office in Munich, later as Sales Manager Europe in the Dutch head office. In 2007 he was appointed as Director of European Cooperative Programs, where he was engaged in several European cluster programs, like the Steering Group Technology of Catrene and as project coordinator for ENIAC projects and two 450mm related FP7 Support Actions. Since last year he is an independent consultant to the semiconductor and semiconductor equipment industry. He is the current spokesman of the Steering Committee of the 450mm Equipment & Materials Initiative EEMI450. He has several patents on his name.

450mm - it's more than abatement, it's the solution.

M. Czerniak
Product Marketing Manager

Edwards, Crawley, United Kingdom

Abstract
Around the time that 450mm wafers enter mainstream semiconductor chip manufacturing, many new process innovations will be introduced, some of which will initially be rolled-out on 300mm wafers first. This paper looks at the implications of these new processes for exhaust gas treatment and the options for managing the challenges these present.

The following will be considered:

III-V transistor channels for high speed and low power - these require the use of flammable hydrogen, pyrophoric metalorganics and toxic hydride gases.

3D memory to increase the packing-density of memory chips - this involves the use of deep etching using potent global warming gases like SF6 which are chemically very stable.

Use of rare-earth metals like cobalt for high-k metal gates - which are harmful if released into the environment.

EUV lithography for producing extremely small features - this requires the use of large flows of flammable hydrogen

CV of presenting author
DR Mike Czerniak, Product Marketing Manager, Exhaust Gas Management, Edwards.

Mike Czerniak received his PhD at Manchester U., and started as a scientist at Philips' UK laboratories before moving to its fab in Nijmegen, working on compound semiconductor applications. He was in marketing at Cambridge Instruments and VG Semicon; he is now the product marketing manager of the Exhaust Gas Management Division of Edwards.

Early production testing of 450mm process modules

M. Cooke
CTO
Oxford Instruments, Plasma Technology, Bristol, United Kingdom

Abstract
The extending timescales for 450mm introduction are causing delays and doubt in the 450mm equipment community. A twin track development approach is proposed that looks for other markets with complementary requirements for some process modules. This enables some of the process scaling to 450mm to be tested, including real production tests, by using single wafer 450mm tools as large scale batch tools for different markets. The possible learning from this approach is discussed, highlighting the gaps that will remain to be tested in a 450mm wafer pilot line.

CV of presenting author
Oxford Instruments has been active in several rounds of ENIAC projects to prepare for the introduction of 450mm, designing modules for 450mm plasma etch and PECVD. Mike Cooke has more than 30 years experience in plasma technology, including plasma source developments, plasma enhanced ALD, and scaling plasma tools. He is CTO for Oxford Instruments Plasma Technology, and has represented the

company in European collaborations.

FOUP (Pod) contamination control solutions for 200mm, 300mm and 450mm substrates.

J. Lundgren
Senior Field Applications Engineer
Entegris GmbH, Microenvironments, Gomersal, United Kingdom

Abstract
Semiconductor manufacturing technologies have developed to the point where small molecules such as water, oxygen and airborne molecular contaminants (AMCs), have become detrimental.
300mm & 450mm FOUPs are designed as controlled minienvironments (MEs) that protect processed wafers from AMCs during storage and transport. However, it has been reported that FOUPs are able to outgas some molecular contaminants (organics particularly) but also to accumulate by sorption molecules outgassed by just processed wafers. Such contaminants are then able to subsequently outgas in the presence of sensitive wafers leading then to detrimental impact.
This cross-contamination scheme from FOUP to wafer was evidenced especially for volatile acids such as HF or HCL and is responsible of yield losses due to drastic corrosion issues or crystal growth on Cu, Al or TiN materials. To better understand cross contamination, different polymers were used in the FOUP's manufacturing and their ability to either induce or control cross contamination was demonstrated. Another AMC control measure is to purge the FOUP with inert gas or to clean the FOUP's using standard DI water cleaning process.

This presentation will highlight the different polymers used in FOUPs for 300mm and 450mm IC manufacturing and the cross contamination risks to wafers from intentional contamination. This presentation will also highlight recent results from contamination control solutions such as purge, DI water cleaning and subsequent contamination effect over time. Measurements are from fluoride contaminated Cu substrates using HF as contaminant since HF is commonly used in several Semiconductor manufacturing processes today.

This ongoing study and research has been conducted, in cooperation and in collaboration with well known research institute CEA-Leti in Grenoble France.

CV of presenting author
Jorgen Lundgren Entegris GmbH Dresden Germany,
Senior Field Applications Engineer with electronic engineering degree from Sweden.
Previously with a Swedish International company for 10 years in a world wide technical support function, whereof 5 of those based in Germany.
Worked for Entegris for the last 17 years supporting the Semiconductor Industry in many different technical roles with focus on wafer and reticle handling, transport and contamination control.
Heading up key projects such as the first 300mm fab in Dresden, European fab conversions, new product qualifications as well as individual customer development projects.
Active contributor to Entegris/CEA-Leti collaboration FOUP polymer contamination/decontamination research Project.
Partner in the Catrene 3D European wafer handling Project.
Active SEMI participant.