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16th European Manufacturing Test Conference (EMTC)

C. Portelli-Hale
SPA Front-End Manufacturing & Technology R&D
STMicroelectronics, , United States

Biography
Chris Portelli-Hale holds the post of Operational Programs Director in the Manufacturing Execution Excellence team within the Front-End Manufacturing & Technology R&D organization of ST Microelectronics, based in Rousset France. He holds a degree in Electronics Engineering from the University of Malta and joined ST in 1989 where he has held various positions is Test Engineering and Test Operations Management within different organizations and locations of the company in Malta, France and Singapore. Chris is Chairman of CAST the Collaborative Alliance of Semiconductor Test group which brings together several actors within the test arena from IDMs, Fabless and Equipment vendors.

A Rapidly Changing Test Landscape

B. Swiggett
Managing Partner
Prismark Partners, Cold Spring Harbor, NY, United States

Abstract
Smartphones, tablet computers and automotive electronics alone accounted for more than one third of all electronics systems value produced in 2013, up from only 13% five years ago. These markets combine high volume production, significant competitive cost pressure, and leading edge IC and sensor packaging requirements. With continuing market growth and device and systems design change, test equipment and production engineers will be challenged to adapt to an ever increasing set of challenges. The emerging "Internet of Things" will also drive significant volumes of low-cost wireless modules and sensors that adapt technologies spawned initially within the mobile and automotive sectors.

This paper will review the key device and packaging trends for mobile and automotive IC and sensor packaging, and will discuss the test and handling complexities inherent in the growth of small form factor SMT and array packages, flip chip and WL-CSP, embedded components, modules and MEMs sensors, and ultimately 3D-TSV implementation. Conventional SMT packages have already reached saturation, and the high volume high complexity consumer-facing segments are rapidly changing the landscape and overall test requirements within the semiconductor supply chain.

CV of presenting author
Brian Swiggett is founder and Managing Partner of Prismark Partners, a thirty-person international electronics industry consulting firm that works at all industry levels from systems to semiconductors. The

company focuses on providing strategic business advice and analysis to companies operating at the leading edge of the electronics industry.

He holds BA and BE degrees from Dartmouth College and its Thayer School of Engineering and has had a wide range of experience in the electronics industry over the past thirty years.

While at Kollmorgen Corporation, his management responsibilities ranged from systems development to manufacturing engineering, product marketing, and operations in the areas of electro-mechanical and electro-optic systems, printed circuit manufacturing and process development, elastomeric connectors, and materials development. He holds several US patents for his work in these areas.

He works with a wide range of Prismark's clients in areas such as semiconductor packaging, system level interconnection and assembly, thermal management, electronic materials, intellectual property assessment, and acquisition strategy.

J. Mai
Managing Director
JEM Europe, Montbonnot-Saint-Martin, France

CV of presenting author
Joe Mai is managing director of the European subsidiary of Japan Electronic Materials (JEM), a leading probe card supplier, for whom he's worked nearly 20 years, playing both technical and management roles in the US and Europe. His technical experience includes R&D, product development, PCB design, automation equipment, and applications engineering. During these past two decades, he has worked closely with many wafer fab customers to improve their test capabilities and develop JEM's technologies.

He is also a program committee member for the SEMI European Manufacturing Test Conference (EMTC).

Using a Test-Cell-Solution Approach to Achieve Device Quality and Production-Efficiency Goals for 77GHz Automotive Radar ICs

P. Cockburn
Senior Product Manager
Xcerra, Test Cell Innovation, Verwood, United Kingdom

Abstract
Radar-based ADAS are moving from 24GHz to 77GHz, providing better range, bandwidth and resolution for detecting objects. Automotive 0 ppm failure rates necessitate full functional test of the ADAS ICs at 24GHz or 77GHz in both Engineering and HVM. Specialized ATE solutions may be under-utilized as requirements change and are not well adapted for HVM. An ideal solution should be usable with different RF and Automotive applications. A co-development between ST and Xcerra has already implemented 28GHz RF test to maintain the highest quality levels. This is based on a flexible test cell base that can be used for other requirements and a system-level solution to maximize OEE and minimize cost. The test cell is now being extended to provide a 77GHz test solution. The DUT has 38GHz IF and several 77GHz TxRx to implement a multiple beam solution for best performance. The device also uses >1 Gigabit serial I/O to facilitate high speed data transfer. The test cell uses a low-cost 6GHz subsystem and optional radar frequency test modules to balance flexibility and cost of full-speed test. An integrated test cell design of the complete signal path, from RF instrumentation, through the fixture and contactor to the DUT, is used to maintain 77GHz signal quality. Production contactors are required for WLCSP and packaged devices. In-socket calibration verifies signal performance at the DUT. Because automotive ICs operate at extended Hot and Cold

temperatures, a "tri-temp" handler ensures the highest test coverage. A systems-level mechanical design enables temperature accuracy of +/-2 DegC. In conclusion, the customer's DUT is tested to the highest levels of coverage, to guarantee quality at the OEMs. The vendor has proven an optimized test cell approach to provide a cost-effective solution with the highest OEE.

CV of presenting author
Peter Cockburn has worked in the ATE industry for over 24 years at Schlumberger, NPTest, Credence, LTX-Credence and now Xcerra. He has developed real-time and GUI software for ATE systems, managed the launch of several SOC ATE systems and new analog test options and provided marketing and sales support in USA, Asia and Europe. As Product Manager in the Test Cell Innovation team, he is now defining new ways to reduce cost and increase uptime when testing semiconductors. He has an Engineering degree from the University of Southampton, UK.

Optimizing Automatic Parametric Test (APT) in Mixed Signal / MEMS foundry

S. Richter
Group Manager Process Control Monitoring
Xfab Mixed Signal Foundry, Erfurt, Germany

Abstract
SUMMARY:
Addresses implementation of improved efficiency in automated parametric test in a manufacturing environment, also across different hardware platforms. Issues to resolve include correlation of tools as well as optimizing test routines for improved throughput and improved accuracy. Describes partnership effort between the device manufacturing and tool supplier.

DETAIL
Test Speed Optimization
o Analysis of the test program (Pareto tool) to identify what the main test time contributors are. Evaluate distribution by test type and test macro. Prioritization of the effort, always 'there is not enough time to optimize the program'.

o Evaluate Fixed range vs Auto range, advantages and disadvantages, speed vs dynamic range trade-offs, compromise is LowRange capability to have dynamic range and speed
o Review standard cases where test program can be optimized

o Review Breakdown tests and optimize for throughput
- Different breakdown tests:
a) WLR style: Gate Oxide breakdown with FN current; more recent "Soft break downs" of GOX detected by the higher noise of the current; qbdrampI, qbdrampI
b) ILD, MOS transistor breakdown; recoverable (MOS) and destructive (ILD)
- differences between Voltage sweep and current force technique

- bv technique, which forces current and monitors measurements to detect various "breakdown" conditions.

- Test conversion from one test environment to another (I.e. different types of testers, or testers from different vendors)
- how to move test information from one environment to another, advantages to stay within close environments, automated scripts to move the data; advantages of "data driven test environments, such as KTE"
- General test requirements: correlation, how to handle and expectations; only parameters that actually characterize the dut/process can be correlated;

- Miscellaneous considerations

o COO
o HV tests
o Using remote testing as a collaborative tool
o Importance of Data sharing between partners.

CV of presenting author

Steffen Richter. Group Manager Process Control Monitoring
Xfab Mixed Signal Foundry, Erfurt, Germany

Steffen Richter was born in 1963 in Germany. He finished his study of Physics and Microelectronic Components at the Chemnitz University Of Technology with degree Diploma Engineer in 1989. He works as Group Manager Process Control Monitoring at X-FAB's R&D department.

About X-FAB Silicon Foundries

As the world's leading foundry group for analog/mixed-signal semiconductor applications, X-FAB creates a clear alternative to typical foundry services by combining solid, specialized expertise in advanced analog and mixed-signal process technologies with excellent service, a high level of responsiveness and first-class technical support.

X-FAB Silicon Foundries worldwide

With its five manufacturing sites in Germany, Malaysia and the USA, X-FAB has a combined capacity of around 62,000 eight inch equivalent wafer starts per month and employs around 2,400 employees worldwide. Sales representatives in major countries in Asia, Europe and in the USA ensure that we stay in close contact with our customers all around the world.

www.xfab.com

CO Author:

Alex Pronin, Applications Engineer Ph.D.
Keithley Instruments, Cleveland, OH, USA

Alex Pronin is currently a lead applications engineer with Keithley Instruments, Inc. in Cleveland, Ohio and has been with the company since 1996. Alex holds a Master's Degree in Physics from the Moscow Institute of Physics and Technology and a Ph.D. in Material Science from Dartmouth.

About Keithley

Keithley, a Tektronix company, designs, develops, manufactures, and markets advanced electrical test instruments and systems for the specialized needs of electronics manufacturers in high-performance production testing, process monitoring, product development, and research.

Keithley has approximately 500 products that are used to source, measure, connect, control, or communicate direct current (DC) or pulsed electrical signals. Product offerings include integrated systems along with instruments and personal computer (PC) plug-in boards that can be used as system components or stand-alone solutions. Keithley customers include scientists and engineers in the worldwide electronics industry involved with advanced materials research, semiconductor device development and fabrication, and the production of end products such as portable wireless devices.

www.keithley.com

Finding meaning in semiconductor manufacturing data using Rich Interactive Test Data Base (RITdb)

M. Roos
Founder
Roos Instruments, Santa Clara, United States

Abstract
A paper by this title is being presented at TestVision 2020 on July 10, 2014. The EMTC paper will provide some of the same information plus a status update.

Emerging products, applications and test strategies are demanding that test data collection and storage become efficient and flexible in supporting new use models e.g. real time or pseudo real time queries, adaptive test and streaming access. The current STDF standard does not support these use models. Hence there is a need in the industry to create a new standard to fulfill these needs. The STDF working group at SEMI/CAST has developed a next generation standard, RITdb, which can support not only the test data logs but other data/information from the test cell.
The effort began by defining RITdb as a simple relational data model to represent STDF, plus mechanisms for storing the resulting tables as files in a RITdb file store along with metadata that can be used to locate files for downstream processing. As part of the effort, STDF to RITdb translators and sample tools for storing and locating files have been implemented. The effort has since expanded to map test equipment configuration information into the same data format, and there are plans to propose standards for ETest data, equipment event information, and an adaptive test interface to testers using the same RITdb format.
A logical architecture based on the standard is being proposed. It includes a standard messaging format for RITdb data that can be streamed in real-time from data sources and uses a broker that supports combining and synchronizing data from multiple sources and delivering it to consumers selectively through subscription. The net result is a plug-and-play data driven architecture. While the overall architecture is a long-term effort, example use cases are provided to show how parts of the architecture can be implemented in the near-term to work with existing tools and applications.

CV of presenting author
Mark Roos is the founder and CEO of Roos Instruments, a position he has held since its inception in 1989. Mark graduated from California State Polytechnic University with a B.S. in Electrical Engineering in 1973 and holds a MS in Electrical Engineering from Stanford University and an MBA from Santa Clara University.

Measurement technology has been the focus of his entire career starting with his early work experience as R&D Project Leader for Hewlett-Packard (later Agilent) Network Measurements Division in Santa Rosa where he was responsible for the microwave receiver and processing (i.e. "bottom box") of the record-breaking HP 8510 Microwave Network Analyzer. After the enormous success of that network analyzer, Mark went on to lead the marketing efforts for HP's RF and Scalar Microwave Network Analyzer products.

The next phase of Mark's career was VP of Engineering for EIP Microwave, a maker of electronic counters and other instrumentation. While at EIP, he discovered a need for high performance automated instruments. He left EIP to found Roos Instruments to serve this market for high-speed RF instrumentation with capabilities suitable for high volume manufacturing.

Early on, Roos Instruments received funding from DARPA via a Small Business Innovative Research (SBIR) grant. The grant allowed Roos Instruments to develop a totally new approach to RF measurements using a single receiver and advanced software -- ideas Mark pioneered. Early in 1994, Roos Instruments won a comprehensive benchmark at Motorola with the RI7100A, resulting in its first major success. Continuing innovate, Roos Instruments introduced Cassini, the first truly modular, high performance ATE. Thus continued Roos Instruments' rise as the supplier of these advanced technologies in production testers world-wide.

Multi-Variate Part-Average-Testing Analysis to Improve Outlier Identification

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Senior Application Engineer
Galaxy Semiconductor , Grenoble, France

Abstract
Microelectronic products produced in a semiconductor fab may be valid in the sense that all their parameters are within the required specification limits but still unreliable in the sense that they have a high probability of early life failure. Such early life failures can be extremely prejudicial in application domains like the automotive sector, for instance.
To screen unreliable products, test programs that were initially designed to check that a product's parameters are within the specification limits, are extended to make specific measurements under varying working conditions. Although this helps to increase product reliability, some early life failures continue to occur. At this point, software techniques are used to improve reliability without increasing the cost of test too much. Basically, such technique called Part Average Testing (PAT), aims to identify valid but unreliable products before they are shipped to the customer by scrutinizing the available test results.
Typical PAT methods used to find outliers consider one test at a time and detect devices whose results (for this test) fall out of a given distribution.
In this work, we consider by contrast parametric methods that operate on the joint results of a group of tests. This "multi-variate" approach is based on the computation of the Mahalanobis Distance that may denote a violation of the correlation pattern between multiple tests results.
The paper gives details about this proposed technique to improve the traditional way of doing PAT, details the software options that were implemented to ease the flow for the end user, it reports on experimental results that were obtained using this technique and finally provides recommendations about possible improvements based on group of parameters which are not linearly correlated.
This paper is coauthored with Jochen Matthias Stefan Product Engineer at Micronas GmbH and Jérôme Kodjabachian Senior Software Developer at Galaxy

CV of presenting author
Nicolas Leblond graduated from INP Grenoble with an Engineering degree, specialized in Microelectronics. He has been working for more than 10 years in the software and semiconductor industries, in startups as well as in larger companies like Xilinx, where he played various roles from design, quality and test to applications.

Outlier technologies ... how to select the right method

D. Hartman
Consultant
TestCIM Consulting, Austin, United States

Abstract
Co_Author: Peter O'Neill, Avago Technologies
The goal of outlier detection is to use test measurement data to identify parts that pass specification limits, but are likely to fail future test steps or to become early failures in the field. Many different methods are available, and most methods are based on parametric measurements, geographic information, or a combination of both. The most common method used is Part Average Testing (PAT) which runs on a test that provides a single measurement for each part in a wafer or lot. Our experience is that this method works well for tests with a normal distribution and which are not highly correlated with other tests. However, in other circumstances, other methods are more effective. For example, if tests have measurements that are very wafer position dependent, methods like nearest neighbor residual and Location averaging improve the separation between outliers and the good population of parts; if tests are pairwise highly correlated, methods

like linear regression offer improved discrimination, and if groups of tests are highly correlated (e.g., IDDQ), methods like Principal Component Analysis work best; if wafers have areas with high defect density, methods that look at clusters work well and if wafers have scratches, scratch detection methods work well. This paper identifies a range of outlier detection methods and provides guidance on when it makes sense to use which methods. The paper also describes software tools that can automatically analyze a collection of tests and select methods to use based on a set of criteria including distribution shape, measurement variation across a wafer, correlation coefficients between pairs or groups of tests, cluster and scratch detection and geographical position within a wafer or a stack of wafers, etc. The tools are recipe based and allow for an engineer to modify the automatic method selection mechanisms based on engineering knowledge of the tests.

CV of presenting author
Current:
- Consultant working primarily for Salland Engineering on software tools to support semiconductor test
- Main focus is Outlier Detection and work with SEMI CAST team to develop standards for test

Work History:
- 16 years at Motorola and Freescale managing teams supporting automation in probe, assembly and test
- 12 years at for AT&T Bell Laboratories doing software development and management

Education:
- BS in Electrical Engineering from University of Texas
- MS and PhD in Electrical Engineering from MIT

R. Segers
CEO
ReSeCo, Veldhoven, Netherlands

Biography
After getting his degree from the University in Eindhoven, Rene Segers started his professional career at Philips. Rene held technical and managerial positions in various divisions from Philips, including Research, Consumer Electronics, the Centre for Manufacturing Technology and Philips Semiconductors which later became NXP. Technically, over the years the focus has broadened from just DfT towards Test and Product Engineering, Diagnosis, DfX and to supply chain management in general. The last couple of years Rene was responsible for the Test and DfX strategy and implementation for NXP.
Rene left NXP in 2009 and is since then active as an independent consultant, supporting mainly smaller companies in developing their business. Rene maintains many contacts in the industry in Europe, Asia and the USA.
Between 1988 and 2004, Rene was also as a (part-time) professor at the University of Eindhoven, teaching DfT and Testing of electronic circuitry.

S. Vock
Principal Test Engineering
Infineon Technologies AG, Test Technology and Innovation, Neubiberg, Germany

Biography
Stefan Vock Biography

Stefan Vock is holding a Diplom-Ingenieur (FH) degree from the University of Applied Science Augsburg and a Master degree in Electronic Systems with distinction from the University of Ulster. He received the designation of European Engineer (EUR ING) in 2009. Mr. Vock has been in the Automated Test Equipment

(ATE) industry for more than 20 years delivering professional services to: ATE vendors like credence and Teradyne, and to design houses as well as to integrated device manufactures (IDM), and today to Infineon in the area test technology and innovation. Further he is currently a Ph.D. candidate at the University of Ulster with the research focus on semiconductor test engineering.

ASIC and SYSTEM tests partitioning for consumer and automotive infotainment markets

D. Dorval
ASIC Operations Director
PARROT, Carquefou, France

Abstract
PARROT is developping its own ASIC products to serve customers and business units in the consumer and automotive infotainment markets.
Thanks to close cooperation and aanlysis, PARROT ASIC and SYSTEM testing groups manage to balance between cost of test, quality requirements, software and hardware constraints and scalability.
We will show how complementary test flows, rapid data analysis and in-depth test knowledge can help to meet our goals of rapid ramp and high test quality to better serve internal and external customers.

CV of presenting author
David has more than 20 years experience in ASIC test development, qualification and ramp-up.
David started his career at Texas Instruments as a test and product engineer from 1995 to 2001.
From 2002 to 2011, he worked for DIBCOM as production director and VP Operations.
Since 2012, David is ASIC Operations Director at PARROT.
David holds a PhD in Physics and worked on CMOS reliability modeling.

Martignoni Stefano

S. Martignoni
Vice President of Worldwide Sales and Marketing
Salland Engineering , Zwolle , Netherlands

Biography
Stefano Martignoni
Vice President of Worldwide Sales and Marketing Stefano is responsible for worldwide sales and marketing for all Salland product lines. Prior to his appointment as director, Stefano was Salland's account manager for South Europe. He brings to Salland over 15 years experience in sales and marketing for the ATE industry. Prior to Salland, he was Senior Marketing director at Credence. He started his career with STMicroelectronics as a product engineer. Stefano holds a Master's Degree from Milan Polytechnics in Electronic Engineering.

MAYOR CEDRIC

C. Mayor
VP Marketing
Presto Engineering, Grenoble, France

Biography
Cédric started in 2000 his career as lead memory design architect on SOI substrate for advanced processor in SOISIC which became a ARM Ltd physical IP department in 2005. From inception he drove the innovation roadmap down to silicon proven circuit memory compilers.

He took over a program manager role in the PHILIPS semiconductor PD, in charge of NPI & Lead Product industrialization in Crolles2 300mm wafer fab from the STMicroelectronics, Freescale, and PHILIPS Alliance. He was involved into yield improvement, process and product transfers to external foundries or within the internal NXP Semiconductors fabs. He successively hold responsibilities in Corporate NXP in Crolles (FR) and Nijmegen(NL)for all the advanced process nodes industrialization, including platform qualification down to 40 nm CMOS technology.

In 2010, he became Vice President for Presto Engineering in charge of DFT innovation & back-end roadmap and strategic marketing, focused on the next generation High Performance Mixed Signal and RF MMW products industrialization needs.

Cédric graduated from Ecole Centrale Marseille in France, and holds a MS of Physics and Electrical Engineering, four patents in the area of chip design and DFM, and contributed to several publication in the field of design and semiconductor test, and productization.

Toffoli Alain

A. Toffoli
Electrical charactrization research engineer
CEA, LETI, MINATEC Campus, DCOS/LCTE, Grenoble , France

Biography
Alain Toffoli is expert in the field of test methodologies.

He received the M.S. degree in engineering from the "Conservatoire National des Arts et Metiers, Paris". He is Head of the Advanced and Statistical electrical characterization Test Team, in the Electrical Characterization and Test Laboratory, of CEA/LETI Minatec-Campus.

His team is responsible of the automated electrical characterizations, for all micro and nano technologies activities and projects. His main research interests include test methodologies.

Semiconductor packaging and test trends: a supply chain challenge'

J.-M. Yannou
Technical Director
ASE, Brussels, Belgium

Abstract
Latest trends in the semiconductor industry are prompting the need for lower power, higher performance,

and greater integration, largely driven by the anticipated proliferation of wirelessly connected devices infiltrating global lifestyles. Poised to constitute the 'next big thing', the 'Internet of Things' is more commonly referred to as IoT, and encompasses limitless applications enabled through scale.
IoT encompasses different devices and end markets, each with their specific market drivers and requirements. But the one resounding driver ultimately required to make IoT happen is integration. Integration is required on many levels, integration of software within hardware, of digital within analog electronics, of digital processing within sensing, and, of RF within power management.
Semiconductors are playing a significant role in enabling IoT. As a result, the industry is seeking ways to develop, streamline and optimize an effective ecosystem, encompassing design, manufacture, packaging and test. IoT is pushing system complexity to new levels, and packaging technologies are being developed accordingly, with innovations in MEMS, sensors and SiP finding particular prominence.
It is recognized that the supply chain needs to evolve alongside technologies. To make IoT mainstream will require a complete and organized ecosystem, as well as a solid supply chain.
As the industry in Europe rises from a downturn decade, this changing environment represents a dynamic opportunity for many European semiconductor design, assembly and test companies.
We will present an overview of technologies developed for miniaturized and efficient modules. We will identify specific technical challenges and emphasize the importance of establishing a strong supply chain, drawing from some pertinent examples. This talk will then explore opportunities within the automotive and sensor segments, particularly as these are both strongholds of the European semiconductor industry.

CV of presenting author
Jean-Marc Yannou is technical director at ASE Group in Europe. Before, Jean-Marc worked in various positions in the semiconductor industry for 18 years. He worked for Texas Instruments in test and product engineering and for Philips (then NXP semiconductor) where he served as Innovation Manager for System-in-package technologies, then for Yole Développement as a senior market analyst.

P. Cockburn
Senior Product Manager
Xcerra, Test Cell Innovation, Verwood, United Kingdom

Biography
Peter Cockburn has worked in the ATE industry for over 24 years at Schlumberger, NPTest, Credence, LTX-Credence and now Xcerra.
He has developed real-time and GUI software for ATE systems, managed the launch of several SOC ATE systems and new analog test options and provided marketing and sales support in USA, Asia and Europe.
As Product Manager in the Test Cell Innovation team, he is now defining new ways to reduce cost and increase uptime when testing semiconductors. He has an Engineering degree from the University of Southampton, UK.

3D IC Test through Power-Line Methodology

A. Pagani
Test R&D and Competitive Intelligence
STMicroelectronics, Agrate Brianza, Italy

Abstract
Today, the main challenge of 3D IC is testing. A mixed signal architecture to test a 3D IC was investigated. This new methodology introduces low complex power line communication circuits to exchange testing signals between ATE tester and at least one chip that belongs to a 3D stack, or between at least two chips.

Significant benefits for probing and 3D DFT access can be highlighted, and some main advantages for using power line communication to test a 3D stack can be:

1) Architecture is fault tolerant for power TSV defects due to multiple TSVs used for each power supply (in order to provide right current to each DUT), then there is TSV self-redundancy that will allow to test 3D DUT in case of some defective power TSVs

2) Architecture simplifies test standardization in particular when in a 3D stack there are chips from different suppliers.

3) Architecture has less constraint at design level regarding routing, because it avoids the introduction of extra test signal TSVs among different ICs of a 3D stack.

Then this new approach has some advantages with respect to other developments in state-of-art. Preliminary studies confirm feasibility of this new methodology applied on standard wafer testing and 3D IC testing through a power line communication architecture.

CV of presenting author
Alberto Pagani received master degree in Electronic Engineering from Politecnico di Milano, Italy. He joined STMicroelectronics in 2000 where he worked for five years in wafer sort department in Agrate as Process Engineer and Test Engineer on Flash memories. Since 2006, he has been working in Europe EWS (Electrical Wafer Sort) and EWS Technology and he is in charge of Test R&D and Competitive Intelligence. He is Member of STMicroelectronics Technical Staff as Senior Staff Engineer. His work is mainly focused on innovative testing and probing methodologies also to develop new products for new markets. He is author of some scientific papers and holds more than 40 patents in several countries.

Cost-effective RF MEMS wafer test solution

E. de Ledinghen
Test manager
Presto Engineering, Caen, France

Abstract
New test challenges
Moving MEMS test upstream to the wafer

RF MEMS have a promising future for cellular phones. The associated test solution will have to manage a sharp ramp up while keeping the final cost as competitive as the GaAs competitor. This paper explains how it is possible to smoothly grow from device characterization to volume test in production.

There is a traditional hurdle between first silicon characterization and the automatic test world. The first one still belongs to designers' team, while the second has already a foot in the production factory. It implies extra cost to bear for start-up companies, because they have to develop and maintain two different test systems: one for evaluation and characterization, and another one for production. It is very difficult to move from one system to the other given the capabilities required by each of them most of the time not compatible (accuracy, turn-around time)
The main idea was here to develop the characterization system, keeping in mind the production test. We decided to select a PXI platform. PXI is easy to program and flexible for the lab, and has also a very low cost compared to traditional ATE. Moreover, we designed also the hardware in such a way that the same interface board can run complex characterization tests and also can be used to evaluate production test and correlate both.
This paper will present economic rationales and technical aspects allowing this solution to claim for the lowest cost and highest scalability for production award.

CV of presenting author
After 10 interesting years developing measuring instrumentation for various industries, and posting 2 patents, Edouard de Lédinghen, today 46 years old, joined the semiconductor industry with Teradyne, the famous tester manufacturer. He helped to introduce new analog instruments before moving to NXP in Caen to put in place high volume production test for RF devices. When St-Ericsson collapsed, he joined Presto Engineering and put in place the new test activity.
Today he drives the fast growing test department and develops Presto offering to lower the cost of test and answer to new requirements from high accuracy analog to 80GHz production test.
Edouard is engineer from ISEP School in Paris. He also enjoys family life with 9 kids !

Trends in Wafer Probing: Challenges and Solutions

J. Mai
Managing Director
JEM Europe, Montbonnot-Saint-Martin, France

Abstract
Successful semiconductor manufacturing is increasingly dependent on test at the wafer level. Some of the main reasons are:
- To avoid the cost and delay of packaging bad devices;
- To eliminate final handler test in cases such as WLCSP or known-good-die (KGD);
- To obtain device characterization;
- To provide in-line, or end-of-line, feedback for process-control;
- To increase test parallelism for higher productivity

However, new device, packaging, and system-integration trends pose numerous challenges for wafer probing.
For example:
- Shrinking device sizes, low-k dielectrics, and high test parallelism require high-accuracy, low-force probing;
- Sensors require physical stimuli, such as light, pressure, magnetic fields, or motion, in addition to electrical inputs;
- Automotive devices (including sensors) require tests over a wide temperature range;
- Higher currents require new probe materials;
- Cu-pillar interconnects require advanced probe cards to avoid pillar damage and to achieve high densities;
- Full-wafer probing (contacting all devices on the wafer simultaneously) is required for low-margin, high-volume devices;

This presentation will attempt to describe the major trends and challenges in wafer probing, and how the probe card industry has responded.

CV of presenting author
Joe Mai is managing director of the European subsidiary of Japan Electronic Materials (JEM), a leading probe card supplier, for whom he's worked nearly 20 years, playing both technical and management roles in the US and Europe. His technical experience includes R&D, product development, PCB design, automation equipment, and applications engineering. During these past two decades, he has worked closely with many wafer fab customers to improve their test capabilities and develop JEM's technologies.

He is also a program committee member for the SEMI European Manufacturing Test Conference (EMTC).

Probe smaller, probe smarter, or how micro-robots can help shorten the development cycle of your products

B. Dagon
CEO and co-founder of Imina Technologies SA
Imina Technologies SA, Lausanne, Switzerland

Abstract
The deep shortage of versatile, multi-domain tools capable of analyzing phenomena occurring at micro- and nanoscales seriously impacts the development speed of advanced semiconductor materials based devices.

In this talk we will present a miniaturized robotic platform which provides capabilities for in situ characterization in both electron and light microscopes. This multi-functional system embeds up to four miBot, our piezoactuated micro robots, allowing the user to independently position the probes over centimeter scale displacements with a resolution down to the nanometer.

These solutions, specifically designed for low current measurements, can be connected with standard third party signal analyzers to carry out electrical characterizations with an excellent signal-to-noise ratio. Moreover thanks of their compact designs, they can virtually retro-fit any microscope setups, even the most tiny ones.

Customer applications and integrations examples will illustrate the advantages of these platforms for a wide range of applications in nanoelectronics, photonics and materials science.

CV of presenting author
Dr. Benoît Dagon currently serves as CEO of Imina Technologies SA, a company he co-founded in 2009. Before that, he conducted a research project at Stanford University and completed a PhD in the field of computer assisted surgery at EPFL Robotics Laboratory. Dr. Dagon also holds a M.S. from EPFL in microengineering with specialization in robotics and industrial manufacturing.

Manufacturing Intelligence and BIG DATA in Real-Time

G. Luhn
Research and Program Manager
SYSTEMA GmbH, Dresden, Germany

Abstract
The increasing availability of information in a connected world is a growing challenge also for the Semiconductor industry. It surfaces in the need for Real-Time information and joined analysis of data from a rising number of sources; ranging from fab to company-wide granularity. That is, manufacturing deciders need granular, Real-Time situational insights to support ad-hoc improvements and decisions. They also require best support for exponentially growing data volumes in testing and production quality control. Overall, Real-Time capability is seen as critical component related to continuous learning and shaping company-wide developments.
Based on thorough research, SYSTEMA GmbH, Technical University of Dresden and SQL Project AG Dresden in cooperation with XFab Erfurt evaluated and analyzed detailed use cases with regard to such challenges. Logical and mathematical analysis led to a new, deeper insight resulting in an innovative conceptual approach toward Real-Time information processing in logistical and technical domains. Known peak phases and bottlenecks of previously applied methods (batch jobs) are becoming obsolete.
Contrary to the common expectation, this approach leads to a simplified system model, which enables maximum algorithmic efficiency and the desired Real-Time behavior at the same time. Any desired data, such as KPIs or statistical data, are continuously aggregated and evaluated, which systematically reduces the required system load while deploying standard software. Ad-hoc value creation and knowledge discovery with the highest degree of parallelization is available using existing hardware (ex.: identification of

dynamically moving production bottlenecks).
An example are continuous quality checks of test results in Real-Time, which is of importance to minimize learning cycles.
The presentation will include a scientific discussion from within the perspective of general Database / Big Data related research activities of TU Dresden.

CV of presenting author
Gerhard holds a Ph.D in engineering science from the University of Erlangen-Nuremberg (Germany). He has more than 25 years of experience in semiconductor manufacturing and information science. Currently, he is heading a program at SYSTEMA GmbH together with the Technical University of Dresden and several major renowned industry partners, which aims at the industrial proof, prototypical and scientific validation of a new, mathematically grounded method of Real-Time information processing, including large data volumes.
Gerhard previously worked as team leader / program manager and research fellow for Infineon/Dresden and Siemens/Munich. He also held various positions in France with Siemens / IBM joint venture in Essonnes; and ST Microelectronics in Crolles.

Recent Advances and Challenges in Nanoparticle Monitoring for the Semiconductor Industry

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Abstract
As presented in the International Technology Roadmap for Semiconductors (ITRS), one of the key challenges facing the yield enhancement community is the determination of process stability vs. absolute contamination levels. This requires data for correlating defects caused by the wafer environment and wafer handling to yield. Ultimately, this will require data to determine control limits for contamination in air, gases, chemicals and ultrapure water. Recent advances in nanoparticle detection in air, gases, and fluids allow the wafer environment to be characterized at unprecedented levels of cleanliness. Data will be presented illustrating the power of the latest contamination monitoring technology to detect nanoparticle contamination events that often occur undetected by conventional monitoring approaches. Determination of contamination in the wafer environment is the necessary first step toward understanding and reducing defects caused by the wafer environment.

CV of presenting author
Dan Rodier is Technology Development Manager at Particle Measuring Systems. He has a Ph.D. in analytical chemistry from the University of Colorado and has over 23 years of experience developing and implementing technologies and strategies to measure airborne molecular species and particulate contamination. Dr. Rodier has four patents for microcontamination monitoring technologies. He has worked with customers across Asia, Europe, and North America to implement monitoring programs in the semiconductor, aerospace, hard disk drive, and flat panel display industries.