Power Electronics Conference

P. Irsigler
Director Technology
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CV of presenting author
Dipl.Ing.Peter Irsigler study at the Johannes Kepler University in Linz physics (1977-1983). He joined Infineon the wafer production in Villach in 1984. He started with process integration for DRAM, CMOS and power devices. Later on he was manager for power technologies and unit processes. Now he is responsible for development, transfers and innovation in the wafer fabrication Villach and responsible for the conversion of technologies to 300mm wafer diameter.

Power electronics key for European industry

W. van Puymbroeck
Head of Unit A4 Components
European Commission, Brussels, Belgium

Abstract
In the More-than-Moore area, power electronics is increasingly important. It provides the necessary components and systems to interface between ICs and the real world, that is more and more electrified. The EU is strongly supporting Research and Innovation (R&I) in this area. An overview of recent projects funded through Framework Programme 7 will be given. These projects range from silicon to III-V based power ICs, including the related interconnect and packaging technologies and cover co-integration of power and low voltage ICs which is essential in many applications. Application areas range from automotive to electrical energy management, with focus on renewable energy management and solar energy conversion. The presentation will also give an overview of new funding opportunities under HORIZON 2020, including through ECSEL.

CV of presenting author
Willy holds a Ph.D in physics from the Universitaire Instelling Antwerpen. He joined the European Commission in the late 80's and throughout his twenty-five year career he has been responsible for research initiatives under different European Framework Programmes. He is the author of several articles in the domain of physics, information technology and integrated manufacturing. Since mid-2011 he is Head of Unit in DG INFSO Nanoelectronics. His responsibilities include Horizon 2020 preparation and stakeholder engagement in the field of electronic components, and the technical, scientific, financial and administrative monitoring of projects.

Technical and economical challenges and stakes of the charge of electric vehicles

S. Cregut
Power Electronics Expert for Charging systems
Renault, Paris, France

Abstract
Renault has started to introduce Electric Vehicle in 2011 with Kangoo ZE, and Fluence ZE , then with Twizy and ZOE in 2012. With more than 170 000 electric vehicle sold, Renault-Nissan group is by far the first group in the world for pure EV makers. Between the different issues and difficulties, improving the charge of the Electric Vehicle is a key point. The presentation will explain in details the expectation of the customers, the different charging modes and the evolutions that are expected in the future. Among the different way of charging, Renault strategy wil be explained, taken into account standardization, future trends, for the different countries (especially Europe- US- Japan and China). To conclude, the expected benefits of large gap components will be discussed.

CV of presenting author
Samuel CREGUT ,PhD in Control Systems works in Renault since 2005. Involved in development of Electric Vehicle programs since the beginning of the EV, he first worked on control of power electronics for EV; he is now the technical responsible of charging System strategy and roadmap.

GaN on silicon: A way to low cost power devices

J.-J. Aubert
Program manager Power electronics
CEA/LETI, DCOS, GRENOBLE, France

Abstract
Silicon based electronic components have been widely used in power electronics since the beginning.
Development of alternative mobility options pushes to prepare more efficient components to answer a growing market with new expectations in terms of performances and costs.
Wide band gap materials have several characteristics that give them real advantages when compared with standard Si technology, such as higher temperature, frequency and voltage operation capacity.
Nevertheless, Si power devices are still very popular and SiC did not take the place. Why?
GaN on Si seems to be a good option to popularize wide band gap components technology since it offers large diameter low cost substrates and full compatibility with silicon technology.
But some of the physical properties of GaN need to set up a specific strategy in terms of power modules to take benefit of the best of the material.
GaN on Si technology will clearly reduce costs of power electronics, enhance technical performance and allow consumers to access efficient products in line with European waste reduction targets for coming years.

CV of presenting author
Jean-Jacques AUBERT recieved its PhD degree from University Joseph FOURIER and Institut National Polytechnique in GRENOBLE in 1978.
He joined LETI in 1979 as a research engineer in material science for the growth of semiconductor crystals for the microelectronics industry.
Envolved in the study of optical materials since 1990, he developed the microchip laser technology and transferred it to the startup NANOLASE.
In 2003, he founded the startup company BEAMIND for the fabrication of contactless probers for the PCB industry.
Back to LETI in 2009, Jean-Jacques AUBERT is now program manager for the materials for nanoelctronics and power electronics

Power Electronics Research in the European ECPE Network - from Power Devices to Systems

T. Harder
General Manager
ECPE European Center for Power Electronics e.V., Nuremberg, Germany

Abstract
ECPE European Center for Power Electronics is an industry-driven Research Network in the field of Power Electronics with about 150 member organisations in Europe, comprising Member companies and Competence Centres. The Network covers the power electronics value chain from the materials and components to the systems and applications.
The presentation will address the following topics:
- Energy saving potential with Power Electronics
- ECPE Network activities including the SiC & GaN User Forum and the ECPE Roadmapping Programme
- Overview and highlights from the Network-internal Joint Research Programme

CV of presenting author
Dipl.-Phys. Thomas Harder

- Thomas Harder, 51 years old, diploma in physics from University of Kiel, Germany
- more than 15 years experience in packaging & interconnection technologies for microsystems as well as multichip and power modules e.g. as a researcher in the Fraunhofer Institute for Silicon Technology (ISIT) in Itzehoe
- since 2003 general manager of ECPE European Center for Power Electronics, the industry-driven Research Network headquartered in Nuremberg (ECPE e.V. and ECPE GmbH)
- since 2006 also cluster manager of the Bavarian Power Electronics Cluster (beside the European Network management)

GaN-on-Si for power electronics: large diameter epiwafers

M. Germain
CEO
EpiGaN nv, Hasselt, Belgium

Abstract
GaN-on-Si technology creates very high expectations for Power Electronics as to provide the next-generation of switching devices. Si switching components are reaching their intrinsic physical limitations, wide bandgap are required to further reduce the losses. The decisive advantage of GaN-on-Si technology to break the Si boundaries for efficient power conversion resides in its excellent and unique combination of performance (breakdown voltage/reduced leakage/lower conducting and switching losses) and cost-efficiency. This mainly thanks to the use of low cost substrates, available in large diameters. Based on more than 14 years of experience in the field of MOCVD-growth of III-Nitrides structures, EpiGaN has established in its dedicated clean-rooms, a unique manufacturing platform supplying GaN epitaxial wafers to the semiconductor industry. As a unique differentiator, the capping of the epiwafers with in-situ grown SiN, is proposed as the optimal surface passivation layer; it enables more robust and more reliable devices. The in-situ SiN passivation further uniquely provides the possibility for reducing transistor dimensions and thus increasing the number of chips per wafer. We'll review the key technical specifications for 650V node GaN-on-Si epiwafers suited for industrial use, today developed on 150mm wafer diameter, as well as latest

developments on 200 mm.

CV of presenting author
Marianne Germain is co-founder and CEO of EpiGaN nv.

She received in 1999 her PhD degree in Electrical Engineering from the University of Liege (BE), where she conducted research in close collaboration with RWTH Aachen, and as invited scientist in Purdue University (US) and Wuerzburg University (D).

In 2001, she joined imec, an international microelectronic research center (Belgium), where she led the development of Gallium Nitride technology for high power/high frequency applications. Since 2004, she became Program Manager of the "Efficient Power/GaN" program, then, group leader of the "III-V systems" group (2007/2010). She also pursued training management course in Vlerick Management School (Gent) in 2008/2009.

In May 2010, with her colleagues, Dr Joff Derluyn and Dr Stefan Degroote, she co-founded "EpiGaN", a clean-tech spin-off, manufacturing GaN epiwafers for electronics applications, where she acts as CEO and member of the Board of directors.

She has authored and co-authored more than 100 international communications. She co-holds several patents in the field of GaN material and devices.

Silicon Carbide devices for high voltage / high current applications

M. Mermet-Guyennet
Programme Director
Supergrid Institute, Villeurbanne, France

Abstract
From scientific and market surveys on wide-band gap semiconductors, SiC devices will mainly find potential applications with high voltage and high current (Voltage Breakdown Vbr >1700V & Nominal Current Inom > 100 A). Among these applications, smart grid, super grid, electricity generation (wind turbine, hydro turbine, and photovoltaic) and traction drive for trains will be the main users of high voltage and high current devices.

The available technology is MOSFET for transistor and JBS for diodes (up to 3,3 kV), some suppliers propose JFET but the trend is mainly towards MOSFET for two reasons : normally-off devices and easy control & paralleling.
For very high voltage 6,5 kV, 10kV, 15 kV and over, bipolar based structure is more relevant and several technologies have been investigated : Thyristors,IGBT.

Another aspect in the introduction of high voltage SiC devices is the global supply chain from the material to the final applications:

1)Base wafers
2)Thick epitaxy (100 m for 10kV)
3)Device processing (choice and design of the structure)
4)Packaging (paralleling for high current, electrical isolation)
5)Integration of gate-drive and capacitor (optimization of switching frequency)
6)Integration of power electronics with sources and loads (cable for grids, motors for traction)

This paper will details some key aspects on the device technologies linked with the applications and the potential solutions for packaging to get high current capability.

CV of presenting author
Michel MERMET GUYENNET is born in 1957. He holds PhD (1984) in Applied Physics from Université de

Marseille-Luminy and is graduated from Ecole Centrale de Paris (1981). He successively worked for Thomson Militaire et Spatial, SGS-Thomson, Advanced Computer Research Institute and Compagnie des Signaux where he had in charge R&D programmes in the field of electronic components and system hardware. He joined ALSTOM Transport in 1996 in charge of technology development for IGBT power converters for traction. From 2001 to 2010, he has been Technical Director of Power Electronics Associated Research Laboratory (PEARL). From 2011 to 2013, he has been in charge of development of full SiC converter with high speed motor. He is now with Supergrid Institute in Villeurbanne as Director of Programme Power Electronics & Power Converters.

SiC and GaN power devices: technologies and products

S. Coffa
R&D General Manager
STMicroelectronics, Catania, Italy

Abstract
Compound semiconductors (and mainly at the moment SiC and GaN) power devices have practically shown a quantum leap in the performances of power devices and in the possibility to enlarge the use of power electronics especially at very high voltages and high power. However, the status of SiC and GaN devices today is much less mature than that of Si power devices in terms of manufacturability, material quality and process control, cost and reliability. In this talk activities on SiC and GaN power devices at STMicroelectronics will be presented.

SiC devices (Power Schottly, MOSFETs) in the fast few years has moved from academic curiosity and outstanding proof of concepts to products with excellent performances and proven reliability. Progress in the quality of substrates and epitaxial layers has been outstanding and evidences will be given on how the screening of residual defects is of paramount importance to achieve high yield and reliability. Also, performances of current products will be presented and roadmaps highlighted.

GaN Devices are also getting out of simple academic curiosity and are promising not only to enlarge the field of use of power devices but also to challenges Si in some of today markets. It will be shown that performances of GaN HEMT devices and the possibility to build them on GaN epitaxial layers grown on Si are opening paths to this scenario. However, especially for high voltage devices (600 V and above), robustness in term of final reliability in the application has to be improved, in spite of the fact that significant progresses in understanding and correcting some of the issues have been made in the last period.

Finally, for both SiC and GaN devices the expected trends of the cost/performances ratio will be presented.

CV of presenting author
Salvatore Coffa was born in Carlentini, near Siracusa, Italy, in 1962. He received a degree in physics in 1985 and a Ph.D. in physics in 1991 from the University of Catania (Italy).

Over a period of more than 20 years in research activity, Coffa has achieved many important research results in various fields and gained key expertise in the area of technology transfer from basic research ideas to prototypes and applications.

In between receiving his academic awards, Coffa pursued a three-year research fellowship from 1986 to 1988 at STMicroelectronics, also based in Catania, and from 1990 to 1992 he was a resident visitor at AT&T Bell Laboratories, New Jersey, USA. In 1993, Coffa returned to Catania to be a consultant for CORIMME, a consortium between STMicroelectronics and the University of Catania, and the following year he became Group Leader within CNR-IMETEM, a laboratory of the Italian National Council of Research in Catania. Latterly, he was the leader of the CNR Silicon Optoelectronics and Micromachining Group.

In 2001, Coffa joined STMicroelectronics as Group Manager, and in September 2002, he was appointed

Director of Research, Silicon Optoelectronics and Post-Silicon Technologies Group, based in Catania and Naples.

Since January 2006 he has held the position of R&D Manager of the Industrial and Power Group (IPG) of STMicroelectronics. With the responsibility for a group of 400 people, Coffa supervises development programs in the fields of power electronics, healthcare, opto-electronics, energy generation (fuel cells and solar cells), and electronics on plastic. He is also responsible for the IPG laboratories for optoelectronics, bioelectronics and electronics on plastic which have been set up in Catania.

Coffa holds several patents and has authored more than 200 publications in international journals. Internationally he is recognized as one the world leaders in the field of Si-based integrated photonics and as an outstanding material scientist. His group interacts with many other companies as well as academic and research institutions in Italy and abroad.

T. Neyer
VP R&D
Fairchild Semiconductor, HV Device Development, Muenchen, Germany

Biography
Dr. Thomas Neyer has received his PhD from University of Technology in Vienna and Cambridge University in 1995. He joined Siemens HL to work on mixed signal Product design and Test. Over the years Dr. Neyer worked on HV and BCD Technologies at Siemens and Infineon Technologies and in 2003 he was entrusted to setup Technology Centers of Competence in Malaysia and China. During the PowerFab start and ramp-up in Kulim, Malaysia in 2005, Dr Neyer was building and leading the Fab engineering and manufacturing teams. Subsequently he was appointed as EVP for R&D and Fab Operation of Grace Semiconductors in Shanghai, China - an advanced Foundry for differentiated, analog Technologies.
In 2011, Fairchild Semiconductor founded a R&D center for High Voltage Technologies in Munich and assigned Dr Neyer to spearhead the effort and coordinate all related Silicon and SiC HV development activities covering device design, modeling and High Power package development.

Market & technology overview of power electronics industry and impact of WBG devices

P. Gueguen
Marketing & Technology Senior Analyst
YOLE DEVELOPPEMENT, Villeurbanne, France

Abstract
Emergence of new wide bandgap (WBG) technologies such as SiC and GaN will definitely reshape part of the established power electronics industry, especially on the high and very high voltage side (>1.7kV) SiC and GaN offer higher frequency switching, higher power density, higher junction T° and higher voltage capabilities (>15kV). To now, the incumbent packaging solution does not fit SiC/GaN specifications. In particular, only a tiny part of the WBG added-value could be captured by using current approaches. Some companies offer a new enhanced package strategy that can help addressing the demand for improved performance, in line with SiC and GaN specifications At midterm, these new power modules could expect targeting a ~$200M market in 2016, exceeding $1B at longer term (2020+).

CV of presenting author
Pierric GUEGUEN is currently working for Yole Développement as a marketing & technology Senior Analyst. He has a PhD in Micro and Nano Electronics from Grenoble INP Institute of Technology , and a Master of

Micro and Nanotechnologies for Integrated Circuits (European program with Grenoble INP/ Politecnico di Torino, Italy / EPFL, Lausanne, Switzerland. He is author and co-author of more than 20 technical papers and 15 patents.
Main knowledge & skills : Power electronics, Power module packaging and assembly technologies, Wide Band Gap devices, 3D-Integrated Circuit (IC) and Packaging processes, Material and semiconductor physics for electronic components, Technological process for micro-nano manufacturing and characterization in clean room
Previous experience : Project Manager on electric vehicles, Vehicle Energy System Division of RENAULT PARIS, Power Electronics R&D Engineer, Advanced Electronic Division of RENAULT PARIS, R&D Engineer, Technical Research Division CEA-Leti (Soitec & STMicroelectronics collaboration) GRENOBLE, FRANCE
His contact: gueguen@yole.fr

Power Electronics - the ultimate path to CO2 reduction

G. Miller
Senior Director R&D
Infineon Technologies AG, Industrial Power Control, Neubiberg / Munich, Germany

Abstract
In a strongly growing worldwide population an even stronger demand for energy is rising - growing from today's tremendous 140*10exp12 kWh per year by further 40% over the next 25 years. At the same time knowing that the exhaust gases set free during energy generation and consumption - mainly CO2 - has to be reduced on values of the 90th of last century, to avoid climatic collapse in the near future. Here power electronics can contribute on many levels starting with electrical power generation out of renewable primary energy (solar, wind, bio-gases), sustaining transmission with lower losses and enabling final consumption with drastically reduced losses. Many examples for the beneficial application of power electronics during the long chain from generation to consumption are shown in the paper combined with underlying principles, numbers and facts. Some examples of power semiconductors with their enabler function to power electronics on their developmental roadmap are discussed.

CV of presenting author
- 30 years of experience in power semiconductors
- Studied electrical engineering sciences focusing on electro physics and semiconductor physics at TU Munich/Germany finishing with a Dr. Ing. in the field of RF- capabilites of power-MOSFETs (SIPMOS).
- 1984 entering Siemens power MOS group
- 1986 project leader of first IGBT development within Siemens with several basic patents and publications.
- 1992 leader of segment IGBT Modules including R&D as a total program manager.
- 1997 leader of discrete high and low voltage MOS- and IGBT- R&D.
- 2005 leader R&D in Infineon's Industrial Power group
- 2008 leader of TI Power in Infineon's Division Industrial and Multimarket with responsibility for SiC and IGBT/Diode technologies.
- 2012 leader R&D technology and Discrete products in division Industrial and Power Control
- 2014 preparing retirement with Enabler and Consulting function in IFX industrial power group.

Progress in Low and Medium Voltage Power Semiconductor Devices.

S. Akram
VP R&D
Fairchild, SanJose, United States

Abstract
Trends to increase power density and performance in Low Voltage (LV) and Medium Voltage (MV) power semiconductors will continue into the foreseeable future with advances in silicon based device structures which remain the workhorse. Advances in superjunction MOSFET and shielded gate trench MOSFETS continue to reduce losses with improve switching performance. In the MV range new materials such as GaN will get introduced into the mainstream application over the next 3 years, driven by the recent progress in this area. These advances in silicon and GaN are being combined with advances in integrated power packaging solutions thereby enabling more efficient systems solutions. This talk will cover the progress in power semiconductor devices in these areas.

CV of presenting author
Salman (Sal) Akram is Vice President of Technology at Fairchild Semiconductor. Dr. Akram leads all semiconductor technology development efforts at the company, including High, Medium and Low Voltage discrete, Analog ICs, EDA and Wafer Level Packaging (WLP).
Prior to joining Fairchild he held senior management positions at Philips and Maxim and served in a variety of engineering and management positions with Micron Technology with over 21 years of experience in the industry.
Dr. Akram holds a Ph.D. in Electrical Engineering from Rensselaer (RPI). He is the recipient of numerous awards an inventor on over a hundred patents, and has published many papers.

Advanced Silicon Substrates for Power Technologies

F. Muemmler
Senior Manager Technology Crystal Growing FZ / CZ
Siltronic AG, Crystal Center, Burghausen, Germany

Abstract
In recent years new Silicon substrates have been developed for power semiconductor devices.
Requirements for these wafers are quite different to wafers for CMOS processes. The presentation will cover various types of Silicon substrates.
As PowerMOS devices are now being transferred to 300mm by first companies like Infineon, Siltronic AG has also developed low resistivity wafers on 300mm. Properties of these wafers and the specific challenges due to the high dopant concentrations are being shown.
For IGBT devices thick epi wafers have been more and more replaced by FZ wafers. Siltronic AG has been ramping up production for 200mm FZ wafers to large volumes within the last few years. Challenges of FZ crystal growth and properties of FZ wafers are being explained.
Due to principle limits of FZ crystal growth, for 300mm IGBTs low Oi CZ solutions are being pursued. The pros and cons of such solutions will be discussed.

CV of presenting author
About the author:
Frank Muemmler is currently Senior Manager at Siltronic AG in Burghausen,Germany for Technology Crystal Growing FZ and CZ. He has been working in this area since 2006.
Main focus is on Crystals for Power Technologies, i.e. FZ Crystals and highly doped CZ crystals with Arsenic, Antimony and Boron doping
2003-2006 Senior Manager Applications Technology at Siltronic AG in Burghausen, Germany

1999-2003 Senior Manager Line Engineering (Process Integration) at Wacker Siltronic Corporation, Portland, OR, USA
1996-1999 Process Engineer Line Engineering at Wacker Siltronic, Burghausen, Germany
1996 Masters degree in Physics, with main subject solid state physics

Smart Power Module and the Future

S. Hong
Sr. Manager, Application Engineering
Fairchild Semiconductor, Motion Control System Team, Rancho Palos Verdes, United States

Abstract
Electrical motors consume about 50% of electrical energy worldwide. Inverterization of motor drive has been the most crucial part in improving energy efficiency. Designing and manufacturing inverters has been getting easier thanks to the progress of intelligent power module which has internal gate driver with protection features. It reduces the total number of components required to build an inverter and improve the manufacturability significantly as a consequence. Intelligent power module from Fairchild, Smart Power Module (SPM), consists of three elements; power semiconductor, drive IC and package. In this article trends and the future of each element will be discussed.
Power semiconductor typically includes IGBT, MOSFET, and diode. Wide band-gap devices are currently being evaluated and certainly will be used in the future. All the development effort has been focused on increasing current density without sacrificing ruggedness.

Field-Stop Trench is the latest technology and has many generations. Short-circuit rating is typically required for motor drive application but at the cost of higher saturation voltage. As over-current protection circuit can sense the over-current situation and respond more quickly, short-circuit withstanding time required for IGBT reduced, and it results in more efficient and cost effective solution. Switching carrier frequency for PWM varies among different applications. There is a trade-off between Eoff and Vcesat, and Fairchild provides two types of SPM optimized for different application needs.
MOSFET has inherent body-diode and can be more cost effective for small power motor drive below 200W. Most of planar MOSFET based module has 500V breakdown voltage rating because die size needs to become 57% larger to become 600V at the same Rdson. Super Junction MOSFET overcomes this limitation by adopting pillar structure. Increased current density on top of 600V rating makes Super Junction MOSFET based module very unique and attractive in some applications.
Reverse-recovery characteristic is the most important aspect for power diode because of EMI concern together with turn-on switching loss of IGBT. Softness is equally important as reverse-recovery time and reverse-recovery current magnitude because it creates Ldi/dt voltage spikes associated with parasitic inductance of the PCB and the package of the module.
High voltage gate drive IC (HVIC) played a significant role in proliferating intelligent power module and inverter solutions. It costs less and easier to put into modules than opto gate drivers, and has been widely adopted in below 7.5kW. Concerns on malfunction and ruggedness of HVIC are being solved. Electrical Over-Stress (EOS) mechanism has been well identified and the necessary measures are being taken. "Power electronics intelligence" will be implemented in HVIC to improve overall system performance.
Package technology requires deep understandings of manufacturing capability and long history of experience. How to minimize the process variation and operational mistakes are key challenges. More robust yet cost effective packages are required. SPM products have various types of packages but mainly there are three groups; Direct Bonded Copper (DBC) package, package with ceramic substrate and lead-frame, and full molded package. PQFN packages are getting popular because of its flexibility and low thermal resistance. Lots of efforts are being made to figure out how to increase power capability and how to make manufacturing easier especially for soldering.
SPM technology and its trends are reviewed in this article respectively in power semiconductor, drive IC and package point of view. Smart Power Module technology will increase its power capability in higher current and voltage ratings. More energy saving can be achieved through adopting inverter more easily with less

cost. The benefit will be appreciated by our children.

CV of presenting author
Steven Hong joined Fairchild Semiconductor in 2011 as a principal application engineer. Currently he is a senior manager in motion control system team. Prior to joining Fairchild he worked for International Rectifier and LG Industrial Systems.
He received a B.S. degree and a M.S. degree (specialized in power electronics) in electrical engineering from Seoul National University. He received M.B.A. degree from UCLA.

Challenges on BCD Technology Evolution

C. Contiero
R&D Senior Director - Company Fellow
STMicroelectronics Srl, SPA FMT-R&D - Smart Power Technology, Milan, Italy

Abstract
Mixed Power technologies like Bipolar-CMOS-DMOS (BCD), represent a good example of the so called "More than Moore" concept where the progress does not depend merely on the evolution of technology node, like in the "Moore's Law" centered on digital, but more on device conception and addition of features driven mainly by application requirements.
The availability on the same platform of a large variety of components to realize high power stages, analog and digital functions, poses many technology challenges to find the best trade-off among the ingredients necessary to guarantee reliable and optimal power device performance and those required to achieve good analog features and large density in the control circuit.
As a matter of fact the roadmap of BCD follows with a few years delay the digital CMOS and the advantages coming from scaling down of lithography are showing saturation on improvement of power device performance.
This presentation will provide an overview about the challenges on BCD technology evolution where to achieve better power devices and added analog functions it requires conception and introduction of innovative device architectures and materials.

CV of presenting author
Claudio Contiero is Senior Director of Process Development and TCAD for Smart Power Technology in STMicroelectronics R&D, Milano, Italy and ST Company Fellow.
He received his Master degree in Physics from the University of Padova in 1976.
He joined SGS-ATES (now STMicroelectronics) in 1978 where he started working on Power Discrete MOS technology. In 1983 he pioneered a new integrated silicon technology called "BCD" that combined Bipolar, CMOS and power DMOS devices on the same chip. Subsequently he contributed to its extension from 20V to 700V and evolution from the 1st (4 µm) to the 9th (0.11 µm) generation.
He is co-holder of many patents and co-author of numerous technical papers on integrated semiconductor power technology.
He served several times as technical committee member of various international Symposia and Conferences, and presented many invited papers. In 2006 he was the "Technical Program Chairman" at the IEEE - International Symposium on Power Semiconductor Devices & ICs.

Smart power technology needs smart substrate

A. Rigny
Business Development Manager
SOITEC, Bernin, France

Abstract
The smart power electronics allows remote control power conversion for real time system optimization. One of the most significant example is the automotive electronics evolution, where more and more mechanical systems (windows, sits, fuel injection, mass air flow sensor, breaks, etc) are remotely controlled through a communication bus (CAN, LIN or FlexRay). The BUS transceiver is a good example of a smart power device that integrates logic, analog and power functions in a harsh automotive environment: voltage spike in the bus of 100V, electromagnetic perturbation that induce noise current, extended temperature range (-40°C to 175°C), while maintaining a very high degree of reliability.

In order to realize such transceiver, the industry has developed a dielectric isolation BCDMOS process, based on a Silicon-on-Insulator substrate (SOI), which consists in integrating power, analog and logic functions onto the same chip in different silicon island to prevent any perturbation. As a consequence, short circuit induced by voltage spike (latch-up) is avoided, as well as electromagnetic induced current noise. The dielectric isolation is also intrinsically temperature independent allowing operation higher than 175°C.

Traditional SOI-BCDMOS process uses a thick SOI wafer (>5µm), shows excellent reliability performances, but with temperature and switching speed limitations. To further improve the performances, thin SOI-BCDMOS technology has been developed, using a thin SOI wafer (~1µm with high uniformity requirement) and based on fully-depleted power device to reduce all parasitic capacitances. The device then shows improved temperature performances, switching speed and low leakage.

The thin SOI-BCDMOS approach brings additional value to the system by improving power efficiency, reducing leakage and system size. And besides automotive, these features are of particular interest in industrial, mobile and emerging applications such as internet of things.

CV of presenting author
Arnaud RIGNY, Buisness Development Manager
Arnaud Rigny has been Business Development Manager since 2011 for Analog and Power application as well as silicon photonics application.
He joined Soitec in 2006 and was managing R&D program between Soitec and CEA-Leti. For several years, he led the customer technical interface for non-digital applications and managed customers in developping new products on SOI and engineered substrates, including imagers, RF, Power and Photonics, working closely with key customers worldwide..
Prior to joining Soitec, he was Product Line Manager at Avanex (prior Alactel Optronics) where he was involved in optoelectronics devices such as pump lasers and Optical add-drops modules. His experience also includes project leader at Corning in optoelectronics device.
Arnaud Rigny holds a PhD and a Master degree in Electronic and Communication from Ecole National Supérieur des Telecomunications at Paris (France).

Power Semiconductors on 300mm Wafers

P. Irsigler
Director Technology
Infineon, Technology, Villach, Austria

Abstract
Energy saving becomes a more and import issue in order to save resources and to lower the CO2 output

worldwide. This is true for all fields of application of power semiconductors starting from electrical energy production, transportation, transformation and point of use conversion. Infineon phases a constant and steady growth in all fields of power technologies. To cope with the growing market demands additional capacities are necessary and have to be built up. To save capital invest and to insure future growth, the idea of 300mm production for power semiconductors was born.
For high power applications the IGBT technology, for medium power applications CoolMOS and for low voltage and power the SFET technology/ SMART technology are used. Several hurdles had to be overcome before starting the first 300mm wafers. The first one was the unavailability of the proper substrate material. The state of the art 300mm wafers for CMOS technologies are p type while all power technologies need to have n type material in all ranges of resistivity. Also the issues of temperature budgets and thin wafer technology had to be solved.
Today all major power technologies IGBT, CoolMOS and SFET are qualified and in production. The next generation technologies will be developed directly in 300mm

CV of presenting author
Dipl.Ing.Peter Irsigler study at the Johannes Kepler University in Linz physics (1977-1983). He joined Infineon the wafer production in Villach in 1984. He started with process integration for DRAM, CMOS and power devices. Later on he was manager for power technologies and unit processes. Now he is responsible for development, transfers and innovation in the wafer fabrication Villach and responsible for the conversion of technologies to 300mm wafer diameter.

Status of silicon carbide substrate production by physical vapor transport method

M. Stockmeier
Deputy Manager R&D
SiCrystal AG, Nürnberg, Germany

Abstract
4H Silicon Carbide has always been a favorite candidate as substrate material for high power electronics due to its wide bandgap, high electric breakdown field and high thermal conductivity. Possible benefits range from improved high voltage switching for energy savings in electric power conversion systems to sensors for harsh environments. Since the beginning of SiC development in the 1990s, the substrate diameter was continuously increased and today substrates with a diameter up to 150mm are commercially available. In parallel, the crystal quality has been improved. Main defect types, like micropipes and polytype conversions, have been markedly reduced and uni-polar devices like SBD have entered mass production. Today, the reduction of dislocations is in the focus of material research. Especially basal plane dislocations (BPDs), characterized by a Burgers vector perpendicular to the crystallographic c-axis, are known to enhance the degradation of bipolar electronic devices.
In this paper, a discussion on recent developments of SiC substrates produced with the PVT process concerning defects as well as diameter will be given. Special attention will be given to dislocations.
Several methods for the evaluation of material properties were applied to determine substrate quality most precisely, e.g. KOH-defect-etching, optical microscopy and high resolution X-ray-diffraction. We found out that several parameters in growth conditions have to be controlled in a proper manner to achieve basal plane dislocation reduction. Based on these investigations we were able to improve our process and the crystal quality significantly. Best values for 100mm 4H substrates show that BPD = 500cm^{-2}, MPD < 0.1cm^{-2} and rocking curve FWHM-values < 15 arcsec can be achieved.

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