## Lithography: What lithography options for tomorrow? (TechARENA)

S. Tedesco
Program Manager
CEA-LETI, Grenoble, France

**Biography**

Biography Dr Serge Tedesco:
1979: PhD in Experimental Nuclear Physics from Grenoble University (F).
From 1980 to 1981: Work on surface analysis equipment development (ESCA) at Riber SA in Paris.
From 1981 to 1987 : Work on electron beam lithography technology at Varian Lithography Product Division in Gloucester Mass. (USA) where he was first responsible for System integration of the raster scan e-beam systems and then Engineering manager .
In 1987 he joined the CEA-LETI laboratories in Grenoble to take in charge e-Beam lithography and consequently all Advanced Lithography activities.
Since 2003 he manages CEA-LETI Advanced lithography strategy and programs as Business Development Manager.
Dr Tedesco has authored or co-authored numerous papers in the field of lithography and he is a Program committee member of the major International lithography conferences. Dr Tedesco has been involved in numerous European projects both as project leader and expert.

## EUV lithography: On the move from pre-production to production

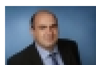
E. Hendrickx
Program manager EUV lithography
imec, Advanced patterning, Leuven, Belgium

**Abstract**

EUV lithography has made gradual and consistent progress over the last years, as currently the first production tools have been installed at the main chipmakers. Some important improvements remain to be demonstrated, but overall the technology is getting closer to pilot production.
Imec started work on EUV lithography in 2006, and from 2008 to 2011 was one of the 2 sites that had an EUV alpha-demo tool operational. Subsequently, Imec was one of the first 2 sites to install an ASML NXE:3100 EUV pre-production scanner, and currently is preparing for the installation of the ASML NXE:3300 EUV production scanner. In this presentation we will review some of the main learnings seen over the last years, give current status of the EUV resists, masks, and scanner, and conclude with the main challenges that still lie ahead before EUV can become fully production worthy.

**CV of presenting author**
Eric Hendrickx graduated from the University of Leuven in 1996, and subsequently was a postdoctoral research scientist at the Optical Sciences Center at the University of Arizona and at the University of Leuven. He joined the lithography department at imec in 2001, and started working on EUV lithography in 2008 when imec started its use of the ASML EUV Alpha-demo tool.

## Mask Less Lithography for Volume Manufacturing



L. Lattard
Laboratory Deduty Manager
CEA-LETI, GRENOBLE, France

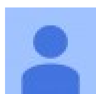
**Abstract**
Besides the development of EUV lithography addressing the high volume manufacturing segment for the production of future CMOS nodes, alternative e-beam lithography techniques are under development and may offer credible and low cost patterning solutions for industry. This paper will review the status of multi-beam lithography technology. This evaluation will be based on the result of the first cluster worldwide installed for multi-beam lithography in CEA-LETI and on tool development in Mapper.

CEA-LETI received the 1st pre-production platform named MATRIX 1.1, and started to evaluate module by module this platform that will operate 1300 beams for an initial throughput target of 1 wafer per hour.

Handling and alignment capability represents two new innovative aspects among the key points introduced in this new generation system. Concerning handling, the development of massively-parallel electron-beam lithography requires strict temperature control and clamping reliability of the wafer during alignment and exposure for the achievement of good overlay performances. The low costs and small footprint of the MATRIX platform does not allow MAPPER to use conventional handling systems. Mapper developed a new type of handling with a Vertical Transfer Robot. To ensure a reliable wafer handling and clamping process, new modules have been developed. CEA-LETI and MAPPER directly investigates the robustness of the different modules in real manufacturing conditions, including the interface of the MATRIX platform with the SOKUDO DUO track. Results on performances in terms of reliability, repeatability and stability will be reported.

**CV of presenting author**
Mr Lattard is graduated from Lyon University in France. After receiving his Master, he worked in the field of flat panel display until 2002.
Starting in 2003 he worked seven years in Germany and he was in charge of process development at Infineon.
From 2009, he is working as project manager in CEA-LETI and is working in collaboration with several tool suppliers for process development on advanced lithography.
Since 2013, he is deputy manager of the lithography laboratory and lead several projects in the field of lithography.

## DSA materials status for HVM



I. Cayrefourcq
Director of Emerging Technologies
Arkema, Grenoble, France

**Abstract**
Since the emergence of microelectronics, lithography has been at the heart of Moore's Law by enabling devices scaling. Wavelength reduction and optics have been the key drivers for such technological feat. This

path remains the preferred one as illustrated by the development of EUV lithography for more than a decade. However, facing complex technical challenges in developing efficient and stable light sources, EUV has been delayed. Therefore, the industry has been extending 193nm lithography by introducing immersion lithography and complex integration schemes, such as multi patterning, at the expense of cost.
In this context, for a few years, Block Copolymer Directed Self Assembly has been considered has a high potential complementary technology to further push 193nm technology. BCP DSA is a disruptive technology based on polymers that self-organize with a period and structure that is defined by the characteristics of the material (i.e: polymer composition defines structure, Molecular weight defines pitch).
In this paper, we will present the state of the art of this disruptive technology and we will demonstrate, through few examples (both at the material and integration level), the readiness of DSA technology for large scale implementation.

**CV of presenting author**
Dr Ian Cayrefourcq is currently Director of Emerging Technologies at Arkema. He is in charge of both Renewable Energies and Electronics R&D portfolios. Before joining Arkema, he has been in charge of various positions including head of R&D departments, Management of large international R&D projects as well as heading a group in charge of New Business Development and Diversification in several high tech companies such as Thales, Corning and Soitec.
Dr Ian Cayrefourcq owns an engineering degree in Material Science, a master Degree in Solid Physics and a PhD in microelectronics. He is author or Co-author of more than 70 publications and 20 patents.

## Nanoimprint status for HVM

M. Wimplinger
Corporate Technology Development & IP Director
EV Group E Thallner GmbH, St Florian am Inn, Austria

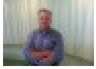
**Abstract**
Nanoimprint Lithography (NIL) has for a long time been praised as the lithography technology of the future. Hopes were placed on NIL as a contender for Next Generation Lithography (NGL) for micro-electronics as a lower cost and less complex alternative to state-of-the-art microelectronics manufacturing technology and more recently EUV on one hand side and furthermore, very generically as a means for low cost, inexpensive patterning at the sub-100 nm-scale. Besides a few very clear target applications such as patterned media (for hard disk drives), the applications needing such patterning capabilities were usually described quite generically without clear boundaries between applications that were better served by conventional lithography and applications where NIL was the better answer. After more than a decade of research in the area of NIL, the technology has reached a level of maturity that enables first applications to transition to high volume manufacturing (HVM) utilizing NIL. This paper reviews the capabilities that NIL provides today and what applications are poised to benefit from those new capabilities. At the same time, the paper also will point out areas where further improvements can assist in enhancing the capabilities of NIL.

**CV of presenting author**
Markus Wimplinger is the Corporate Technology Development and IP Director at EVG. In this role, Markus oversees EV Group's global Process Engineering team. His further responsibilities include the management of R&D partnerships and contracts with 3rd party organizations such as companies or government related entities, as well as Intellectual Property affairs associated with EVG's process technology development efforts.

Markus received his educational background in Electrical Engineering from HTL Braunau, Austria. He started with EV Group as a project manager at the company's headquarters in Austria in 2001 with focus on customer projects. In 2002, Mr. Wimplinger transitioned to EV Group North America in Tempe, Arizona, USA, where he served as the Director Technology North America till August 2006. Mr. Wimplinger's past work includes involvement in design, development, process technology and many other aspects of capital

equipment production at both EV Group and at his former job with a capital equipment supplier for non-semiconductor related industries.

## Increasing Efficiency and Effectiveness of Processes in Lithography Related to Airborne Particle Measurement



A. Jackson
Field Application Engineer
CyberOptics Corporation, Golden Valley, United States

**Abstract**
Stringent manufacturing requirements and the need to maximize both yields and tool uptimes for Photo Lithography Applications requires best-in-class practices for a contamination-free process environment. Quickly identifying when and where airborne particles originate and the source of the contamination is challenging with traditional surface scan wafer methods.
Whether for equipment diagnostics, particle qualification or preventative maintenance, equipment engineers need to identify and troubleshoot airborne particle issues efficiently and effectively. Legacy methods are not real time, may cause long delays for results and are costly in terms of downtime if required to tear down the fab tool or run a series of test wafers. Legacy methods also lead to delays in equipment qualification, equipment release to production and maintenance cycles.
CyberOptics will review the advantages of using the wireless wafer-like real-time particle counter method to locate and troubleshoot airborne particles with the ReticleSense Airborne Particle Sensor (APSR) in reticle environments. This solution can quickly check the dozens of particle sensitive chambers that otherwise might take days to check with multiple surface scan wafers.
Along with the ParticleView software, particles are recorded to compare past to present as well as tool to tool. APSR follows the Reticle path and can travel to multiple areas of the tool to precisely and accurately detect where particles fall. APSR measurement devices are capable of detecting and counting particles as small as 100 nm (0.1 micron) and transferring accurate real-time data wirelessly to a PC with graphical and numerical analysis. Tests or calibrations can be conducted under production conditions for seamless ease-of-use.
The APSR solution improves yields, optimizes maintenance and increases equipment uptime compared to legacy methods. Specific time and cost savings will highlighted.

**CV of presenting author**
Allyn Jackson is a Field Application Engineer for CyberOptics in the US and Europe. Allyn works closely with equipment and process engineers at major semiconductor fabs and equipment OEMs.

His extensive expertise includes collaborating on evaluations and providing training and technical support for wireless semiconductor measurement devices that are used for chamber gapping, leveling, wafer handoff teaching, vibration and airborne particle measurement.

## Advantest F7000 leading e-beam lithography tool

S. Ainslie
Director Business Development
Advantest Europe GmbH, Munich, Germany

**Abstract**
Authors: Takayuki Nakamura, Kiichi Sakamoto, Masahiro Takizawa, Stuart Ainslie

Advantest 's F7000 e-beam lithography tool is equipped to meet the wide demands of the semiconductor

industry offering high resolution, enhanced through put and high availability. The tool can be used to write wafers or masks.

Addressing the needs of advanced R&D the lithography tool is mask less and can write leading edge structure sizes in the 1x nm range achieving smooth edges and good accuracy. Introducing variable shaped beam and character projection capabilities the tool is versatile to write diverse and complex shapes while achieving leading through puts.

F7000 has been engineered to achieves highest uptimes and offer high utilisation. The tool has unique self-cleaning capabilities and requires reduced preventative maintenance to be carried out.

**CV of presenting author**

Biography Stuart Ainslie:

With over 25 years experience in the semiconductor industry Stuart Ainslie has been with Advantest for 19 years and is currently Director of the business development group located in Munich.

In Advantest Stuart worked as an applications engineer before joining the marketing group in 2000. Stuart originally studied Electronics and Electrical Engineering in his native Fife Scotland and in 2008 was awarded an MBA from the Open University (UK).

Stuart is married with two children and lives in Munich.