Exhibitor Presentations: Packaging (TechARENA)

Biography
Ourania Georgoutsakou joined SEMI as Director of Public Policy for Europe in October 2012, with the role of liaising between SEMI members and European, national and regional decision-makers to reinforce cooperation between industry and public authorities in the interest of a globally competitive Europe semiconductor value chain. She has 10 years of experience in European policy-making processes and advocacy, gained as Senior Policy Coordinator for the Assembly of European Regions (AER), the largest independent network of regional politicians in Europe. She has worked on such diverse policy areas as the EU institutional set-up and the Lisbon Treaty, and EU health, social, innovation, competition and cohesion policy. Ourania holds postgraduate degrees in EU Law and in EU policy-making and lives with her family in Brussels.

Solutions for thinning, dicing and packaging of power devices made of Si, Sapphire, SiC and GaN

G. Klug
Sales Manager
DISCO HI-TEC EUROPE GmbH, Munich, Germany

Abstract
Wafer thinning and dicing are essential processes for manufacturing semiconductor products.
DISCO Corporation is a leading manufacturer for equipment and tools for wafer thinning and dicing. "Bringing science to comfortable living by Kiru (Dicing), Kezuru (Grinding) and Migaku (Polishing)" is DISCO's mission. By combining these three core technologies, DISCO provides total solutions to meet the more and more demanding requirements of the semiconductor industry in terms of manufacturing thin dies with high die-strengths and several new approaches for advanced packaging. When developing such processes, circumstances for the total process flow from front-end to packaging are actively taken into consideration.
We are going to introduce various technologies for thinning, polishing and singulation (dicing) of wafers made of Si, SiC and GaN. Further the technologies of planarization for Cu-Cu bonding, planarization of tape and a process for via hole drilling for interconnecting dies to other dies or substrates are described.

CV of presenting author
Gerald Klug studied business engineering at the University of Siegen and graduated in 1998 as Dipl.-Wirt.-Ing., completing his thesis at BMW in Munich. He started his carrier as a designer of coil processing lines for nearly 3 years at a German machine manufacturing company, Heinrich Georg GmbH. At the end of 2000, he joined DISCO as a Sales Engineer for the area of Scandinavia. Meanwhile he has been almost 14 years at DISCO, currently Sales Manager in charge of major customers in Europe.

TLS-Dicing - Enabling technology for separation of SiC wafers

H.-U. Zuehlke
Market Development Manager
3D-Micromac AG, Chemnitz, Germany

Abstract
The new TLS-Dicing (thermal laser separation) tool microDICE from 3D-Micromac AG is an enabling dicing tool for new products and materials. The tool helps to overcome several disadvantages of known dicing technologies like chipping, pealing of backside metal or thermal induced defects. Even SiC-based products can be separated with low costs, no tool wear and with very high throughput.

In the microDICE tool thermally induced mechanical stress is used to separate brittle materials [1]. TLS-Dicing is a one pass cleaving process and runs with up to 300 mm/s (also for SiC!). Brittle materials like wafers are separated by thermal induced mechanical stress. Hence front and backsides are free of chipping. Back side metal, as typical for many SiC and Si-power devices, is separated in the same step with no delamination and very smooth edges. Metalized patterns inside the dicing street can be removed by using the scribing laser without influence on the throughput. TLS-Dicing has no negative thermal impacts on the separated devices, proved by electrical measurements of leaking current [2].

The presentation covers an introduction to the technological principle of TLS-Dicing technology with special consideration of SiC-wafers. Typical application results will be presented. An overview on the modular and in terms of throughput and cost scalable microDICE tool architecture will be given. The presentation will be concluded with a consideration on the aspects of throughput and cost of ownership for a typical SiC-wafer project.

[1] H.-U. Zühlke: "Thermal laser separation for wafer dicing"; Solid State Technology, 2009

[2] D. Lewke et al.: "High quality and high speed cutting of 4H-SiC JFET wafers including PCM structures by using Thermal Laser Separation"; MRS Spring Meeting, 2014

CV of presenting author
Hans-Ulrich Zuehlke studied instrument engineering at Friedrich Schiller University Jena. In 1998 he received his PhD from this university. He has active more than 15 years experience in the laser business. Last ten years in the field of laser applications for the semiconductor industry. Beginning of 2014 Hans-Ulrich Zuehlke joint 3D-Micromac AG Chemnitz as Market Development Manager for semiconductor equipment.

New WLP-Technology-Fusion Concept Offers Significant Advantages

S. Kroehnert
Director of Technology
NANIUM S.A. - Niederlassung Dresden, Technology / Technical Marketing, Dresden, Germany

Abstract
NANIUM has developed a new advanced packaging solution for classical Fan-In WLP/ WLCSP, applying its leading edge Fan-Out WLP/ eWLB knowledge and HVM capabilities. Independent of the incoming wafer diameter, a new standardized 300mm reconstituted mold wafer is built with the Known-Good Dies (KGD) of those incoming wafers only. The dies are placed with very small distance to each other. That way two 200mm wafer or even four 150mm wafer can be WLP processed on one reconstituted 300mm mold wafer. This is giving significant cost advantage, depending on the incoming wafer diameter and die size. This new WLP-Technology-Fusion concept is called FIMP (Fan-In with Mold Protection), as the Fan-In/ WLCSP dies

will have molded backside- and sidewall protection around the die after final package singulation, which makes it more robust for handling and operation. All the routing and bumps are placed on the die itself, so it remains a Fan-In WLP/ WLCSP solution. The molded sidewall protection in fact could be seen as very small Fan-Out area, which in that case is not used for routing and bumping. Besides the cost aspect, the FIMP concept is important for advanced CMOS technology nodes using Low-k and ULK materials. Wafer probe can be applied to already singulated dies, now embedded in the reconstituted mold wafer. This allows to test also for Si wafer dicing fails, which are more critical in advanced CMOS technology nodes, requiring new dicing methods like laser grooving. This has been possible so far only by expensive and inefficient WLCSP bare die handling and testing. Final package singulation of the reconstituted mold wafer is done by dicing of mold compound, while the singulated and tested Si die is protected.

CV of presenting author

Dipl.-Ing. Steffen Kröhnert received his master degree in Electrical Engineering and Microsystem Technology at Technical University of Chemnitz, Germany, in 1997. In the same year he started his professional career as Development Engineer in the Corporate Package Assembly, Interconnect and Test Development Center for Semiconductors of Siemens AG in Regensburg, Germany. After carve out of the Semiconductors Business Unit to Infineon Technologies AG in 1999, he worked as Project Manager and moved to Infineon Dresden GmbH & Co. OHG in 2002 to support local setup of Package Development Department for Memory Products. He became R&D Area Manager Component Development and took over Technology Platform ownership for FBGA products. From 2006 he was working as Senior Manager in Qimonda Dresden GmbH & Co. OHG, the carve out of the Memory Products Business Unit of Infineon Technologies. Begin 2007 he was assigned to Qimonda Portugal S.A. to setup and lead Package Development team at volume production site. Since 2009 he is Director of Technology at NANIUM S.A. in Vila do Conde, Portugal. Steffen is author and co-author of 23 patent filings in the area of Packaging Technology. He is member of IEEE CPMT, MEPTEC, SMTA, VDI, VDE and GPM. He contributes as Technical Committee member to SEMI Europe Advanced Packaging Conference (APC) and Electronics System Integration Technology Conference (ESTC).

Advanced Packaging related lithography challenges

P. Cochet
Director, Technical Account Management
Rudolph Technologies, Wilmington, MA , United States

Abstract

Semiconductor packages must be thin, small and cost-effective which is a given in the semiconductor back-end industry. Packaging today plays a critical role when it comes to device and system performance. Many different advanced packaging approaches are being pursued.

If all processing and manufacturing infrastructure for Si are already established in semiconductor facilities, Si interposers today are built on mature front-end lines which makes manufacturing very expensive, hence the search for alternative integration technologies such as those based on fan-out wafer level packaging or alternative interposer materials. Glass, for example, offers benefits with its ability to match TCE while exhibiting significantly improved electrical characteristics, critical for high-end, high-frequency devices. Common interposer manufacturing processes are comparable to wafer level advanced packaging processes. Metal seed layers have to be patterned and etched. Plating molds need to be defined either in thick photoresist or in dielectric materials. 2.5D interposers also require processing of redistribution layers (RDL) on both sides which tends to impact the physical behavior of wafers or substrates with warpage.

This paper specifically lists the various lithography challenges which are being encountered when manufacturing high density 2.5D interposers. Typical back-end litho requirements regarding resolution, overlay, sidewall angle and depth of focus are discussed. In addition, the application-specific litho challenges such as a large exposure field size and IR backside alignment capability for TSV or TSG are reviewed.

As with all back-end processes, interposer manufacturing must be extremely cost efficient and high yielding. A middle ground between costly front-end processes and more robust and lower cost back-end processes

has to be found. This paper also discusses potential cost reduction via economy of scale with a cost model for glass interposer manufacturing on large panels.

CV of presenting author

Philippe Cochet is the Director, Technical Account Management at Rudolph Technologies which acquired Azores Corp in 2012 where he hold the position of Director, Business Development. Mr. Cochet has 30 years of sales, marketing and customer service experience and hold different positions at Zeiss SMT, Accretech, Zygo, Fairchild Technologies and at GCA (19 years), a photolithography capital equipment manufacturer. Mr. Cochet hold degrees from the university of Montpellier.