Exhibitor Presentations

Plasma etch and deposition solutions for SiC and GaN devices

M. Dineen
Technical Marketing Manager
Oxford Instruments Plasma Technology, Strategic and Product Management, Bristol, United Kingdom

Abstract
Silicon Carbide (SiC) and Gallium Nitride (GaN) are becoming increasingly important materials for RF and Power devices.Find out how plasma process solutions are used to enable these devices and maximise their performance.

Biography
Dr Mark Dineen graduated from Cardiff University with a PhD on ‘Plasma etching of Gallium Nitride’ and joined Oxford Instruments in 2000. Firstly as a Process Engineer working on etching of III-V materials, then moving into Product Management and more recently marketing Mark has a wealth of experience related to Compound Semiconductor device processing.

Atomic layer deposition for 3D objects and MEMS

C. Hossbach
General Manager
Picosun Europe GmbH, Dresden, Germany

Abstract
d objects and MEMS

Atomic layer deposition (ALD) is superb method to deposit high quality thin films to challenging structures. It provides uniform, conformal coatings of various materials, for example many metal oxides, nitrides and pure metals. It does not require line of sight, so even pipes or microfluidic channels can be coated from inside. The growth is digital, so thickness is well controlled and the films do not have pin-holes. Therefore it is popular approach to passivate and protect parts from nanodevices to large machine parts. ALD films are also used to tune electrical (insulating and conductive layers), optical and mechanical properties and for encapsulation.
ALD is widely used in microelectronics and Moore's law is nowadays depending on ALD. E.g. modern logic and memory devices rely on ALD processes. The use of the method has also gained more and more attention and new applications have been found outside the traditional field of use. Picosun ALD process is for example used in coating of medical devices, luxury watch parts, collector coins, machine parts, medicine, batteries, automotive components, pipes, bottles and even complete mobile phones. The traditional field of coating semiconductor wafers has expanded to MEMS, LEDs, compound semiconductor devices, photonics and to different sensor and detector fields.
Picosun will present the examples how our customers can benefit from ALD technology. And if you think carefully, you will be able to find a part in your process which would benefit from atomic layer deposited films.

Biography
Dr. Christoph Hossbach obtained the Dr.-Ing. in Electrical Engineering in 2013. Since 2017 he is General Manager at Picosun Europe GmbH responsible for Germany, Austria and the Netherlands. Earlier he worked as a Senior Scientist at TU Dresden, IHM. His fields of expertise include Atomic and Molecular Layer Deposition, Chemical Vapor Deposition, metrology, as well as tool and component design. Dr. Hossbach is co-founder of ALD Lab Saxony and was involved in teaching and consulting.

Optical inspection key for functional test, validation and qualification for 3D sensing and lidar

J. Sprankenis
Manager New Business Development
NTS Optel, Sales, Eindhoven, Netherlands

Abstract
In the growing market of Photonics, optics, opto-mechatronics and opto-mechanics customers demand a high very high quality standard with 100% quality products delivered.

This means that every single products needs to be tested and validated.

NTS Optel is, for many customers, the partner of choice for the delivery of manual or automated optical measurement solutions for optical inspection, functional testing, validation and qualification. Markets we are involved are 3D sensing and lidar.

3D sensing and lidar can be achieved using a number of different technologies. The most used technologies in this fast growing market is stereoscopic imaging, structured Light Pattern and Time of Flight (ToF). Each of these technologies has its common use cases and individual strengths.

From the beginning of the first commercial 3D sensing product “The Kinect gamecomputer” we were involved in the 3D sensing revolution.

The industry picked up this game changing technology and created al kind of new applications. For example 3D sensing in mobile phones on robots.

We are specialized in develop and building customized testers for optical testing of passive and active optical devices such as DOE’s, MLA,s, Wafer Level Optics (WLO) and VCSEL’s on component level but also sub- and complete packaged modules like IR laser projectors, structured light laser projectors, Time of Flight (ToF) sensors, LIDAR, illumination and projection modules.

With 30 years of experiance we are the partner of choice of leading customers. With development and realisation of the systems under one roof we are a one stop shop organisation ready for your challanges.

Let's work together and accelerate your business!

Biography
Background: Precision Mechanics, Mechatronics, opto-mechatronics and optical engineering.
Sinds 2009 working at the NTS group in severall positions. Now responsible for the business development with NTS Optel.

In the presentation we will zoom in at severall project examples, expertise, what we measure etc.

The Art of Dispatching: Dealing with today's Complexity in Manufacturing

R. Walter
Managing Director Systema Asia
Systema Systementwicklung Dipl.-Inf. Manfred
Austen GmbH, Dresden, Germany

Abstract
Multiple process steps and countless influencing factors create highly complex and often interdependent scenarios that are simply too complex for manual dispatching. With factories already running at maximum capacity, manufacturers look to take the friction out of their operations. In order to optimize equipment utilization while handling complex inventory and bottleneck feed and line balance issues, a tightly integrated dispatching software enables improved equipment loading and throughput.

This presentation briefly introduces the new aspect of "process capabilities" and summarizes a real time dispatching solution based on event driven optimization.

Biography
• Managing director SYSTEMA Automation Solutions Malaysia
• About 20 years in semiconductor industries
• Strong understanding of manufacturing challenges and industry trends
• Trusted advisor for Manufacturing Operations Management

Yield Improvement by Abrasion Reduction

J. Lundgren
Senior Field Application Engineer
Entegris, Dresden, Germany

Abstract
This presentation will describe different polymers and their technical attributes and functions in products used for bare die and wafer handling and processing applications.
Polymers used in wafer handling and processing has to have a low level of organics which can potentially outgas (outgasing) and low level of anions, cations and metals. Some polymers are required to have ESD (electro static dissipative) properties where different forms of carbon is added to achieve the required ESD specification. Another critical physical attribute is abrasion resistance. Specific polymers have a high abrasion resistance to avoid particle generation. Temperature resistance is another important factor for many Semiconductor applications.

Biography
Senior Field Applications Engineer with electronic engineering degree from Sweden.
Been working for Entegris for the last 21 years supporting the Semiconductor Industry in many different technical roles with focus on wafer and reticle contamination control during handling, processing and shipping of sensitive devices.
Heading up projects and product qualification of 200mm and 300mm fabs in Europe.
Contributor to Entegris/CEA–Leti collaboration FOUP polymer contamination/decontamination Project.
Partner in the European TSV-Handy wafer handling Project.
Active SEMI participant.

Extend the lifecycle of your industrial IT systems > 20 years

R. van Hagen
Business Development Manager
Detron Lifecycle Services, Veenendaal,
Netherlands

Abstract
IT components like servers, IPC systems and boards that are used in the semiconductor industry should be robust, secure and of high and constant quality. In addition, systems are used over a longer period of time and redesigning an alternative product results in additional cost and risks. During this presentation, Detron gives insight in its Lifecycle management strategy that helps customers like ASML, Philips and NTS choose/design-in the right IT components and extend the lifecycle of these products for more than 20 years.

Biography
Robbert van Hagen has a strong 20-year background in ICT managed services both in the IT and Telecom domain, acting as a sparring partner in the field of mobility, Internet of Things and Lifecycle Management.

Quality Assurance in High-End Semiconductor Production

M. Holzapfel
Business Development Manager Semiconductors
Precitec Optronik, Neu-Isenburg, Germany

Abstract
PRECITEC is worldwide the preferred supplier and partner of high-end standard and customized optical sensor solutions for quality control in production processes of semiconductor and consumer electronics. Using our non-contact and non-destructive technology, deviations in essential steps of the manufacturing process can be detected. Thus, we enable not only a significant increase in the quality of subsystems and finished goods, but also a reduction of time and cost in the assembly processes.
PRECITEC equipment is currently used in application scenarios in the semiconductors such as:
• In-process wafer thickness measurement (grinding, CMP, etc…)
• Fast warpage inspection
• Bumps and micro-bumps inspection
• Laser dicing groove inspection
• In process dicing laser autofocus
• And many others

Biography
Mathias Holzapfel is a Business Development Manager at Precitec Optronik with a focus on the Semiconductor industry. His responsibility encompasses Precitec's worldwide Semiconductor sales.

Upon completing his engineering degree in "Photonics and Image Processing" Mathias began his career as a technical sales and applications engineer in the field of diode array spectroscopy. Later he moved on to industrial image processing were he further developed his software and application expertise. These skills and experiences lead him to his current position at Precitec Optronik.

Non-contact metal layer thickness and sheet resistance measurement on process wafers

M. Klein
Managing Director
SURAGUS GmbH, Managing, Dresden, Germany

Abstract

Thickness measurement is a crucial yet challenging endeavor in many industries. Processes such as sputtering, plating, polishing or selective etching among others benefit from instant metal thickness measurement. To date, indirect measurements on test wafers often lead to uncertainties resulting from a selective measurement of samples. They also cause additional costs for processing test wafers and consuming tool time. Furthermore, high-resolution measurement near edges enables integrity assessment of near edge areas. These near edge areas receive broader attention these days as they still provide significant potential to increase the yield and decrease costs per chip.

Novel tool integrable measurement technology is required to adapt to these challenges and to assure accurate, non-contact and reliable measurements of the layer thickness even at high wafer handling speed. Therefore, non-contact sensors for intool monitoring and detailed offline imaging have been developed based on eddy current technology, a well-known method for layer characterization, and have been adapted to the challenges of in process and edge area measurements. A sophisticated evaluation enables a precise interpretation of the obtained data, including near edge areas. It is shown that the received results are equivalent to destructive thickness and contact 4PP measurements. Eddy Current, though, is a much faster method. In contrast to other approaches, this non-contact method erases impacts of insufficient homogenous contact qualities and therefore leads to a higher repeatability. Examples will be given where the eddy current measuring method has been applied on top of structured multi-layer systems or obtaining precise thickness measurement near edges.

This talk is dedicated to initiate a discussion on the shift from measurement on test wafer to measurement on process wafers.

Biography

Dipl.-Wi.-Ing. Marcus Klein has been managing director of SURAGUS GmbH since 2010. He got his master degree in Business and Engineering from University of Technology Dresden focusing on microelectronics and electronic packaging. Past working experiences include Siemens Pte Singapore, Wacker Chemie, Advanced Mask Technology Center and Fraunhofer Institute for non-destructive testing Dresden. He is member in several research projects and expert for eddy-current based measuring solutions for thin films, coated glass, carbon fiber and graphene.

Maintenance Management 4.0

J. Kinauer
Director Channel Sales
camLine GmbH, Sales & Marketing, Petershausen, Germany

Abstract
Highly productive, profitable manufacturing must also focus on the automation of maintenance in order to work efficiently, flexibly and sustainably. The purpose of intelligent maintenance is more than just organizing the maintenance staff! - It must analyze process data for predictive maintenance, observe the material flow, keep spare parts, coordinate the maintenance staff and, of course, document maintenance activities. In addition, it is important in a complex production with large plant inventory that the maintenance measures and experiences are documented as best-known methods (BKM).

There are different maintenance methods like corrective, predictive or preventive maintenance. Each maintenance type may be used at specific occasions, depending on the impact to the life time of the equipment and production. Predictive Maintenance as the most complex maintenance type requires that equipment data is analyzed with statistical methods like Western Electric rules.

About camLine
camLine (camLine.com) develops and markets its own software providing powerful solutions to the challenge of "Manufacturing Excellence" in the MOM sector. camLine's IT-based infrastructure systems are used in the manufacturing of high-tech industries. camLine's priorities are quality assurance with SPC/APC/SQM, process integrity with a recipe management, production logistics, efficiency (OEE), shop floor integration, engineering analytics, machine maintenance, and innovation efficiency. Training and consulting is provided by camLine's own academy. camLine has been offering its services worldwide for more than 29 years.

Biography
Jochen Kinauer currently serves as Director of Channel Sales and Public Relations at camLine GmbH. In his career, Jochen was responsible for SW Automation Projects for Semiconductor Manufacturing, which includes MES, Equipment Integration, Tool Controls, FDC, APC and SPC.

In addition Jochen Kinauer serves as Cluster Manager at Silicon Saxony e.V. for the cluster Advanced Semiconductor Manufacturing Technologies and RFID. As part of his role Jochen organizes an annual RFID Symposium in Dresden, showing new developments and technologies in the area of RFID and Indoor Material Tracking that takes place every year at the beginning of December in Dresden, Germany.

Siconnex BATCHSPRAY Technology: Case studies for cost- and space improvements

F. Wörndl
Global Director Sales & Marketing
Siconnex customized solutions GmbH, Sales, Hof bei Salzburg, Austria

Abstract
Siconnex BATCHSPRAY technology is used, if a high throughput on a small footprint, as well as a low chemical consumption matters.
In a case study, that was done together with a European customer, the benefits of moving from a wetbench or single wafer track to a BATCHSPRAY equipment in terms of money and cost savings are shown.

Biography
Fabio Wörndl started at Siconnex in 2011 as Service Engineer. After a technical sales support role for the US market, he became Account Manager in 2016. Since July 2017, Fabio is Global Director of Sales & Marketing at Siconnex and manages the sales structure around the globe.
Fabio has a degree in electronics and a diploma in industrial engineering and economics.

Scaling up to big data volumes

D. Suerich
Product Evangelist
PEER Group, Kitchener, Canada

Abstract
The market is demanding faster throughput, smaller feature sizes, and higher quality. The fuel that drives these improvements is data – from more sensors, faster sampling, and greater integration of different sources. Collecting larger data volumes allows for deeper insight into critical process and production metrics, as well as the possibility of using advanced analytics and machine learning to speed defect analysis and reduce repair times. However, this explosion of big data can overwhelm traditional data sharing and storage mechanisms. Join us as we discuss cutting edge approaches to managing your data including new storage solutions, best practices for where your data should live, and methods for sharing that data with your analysis systems and global experts.

Biography
Doug Suerich is Product Evangelist at The PEER Group Inc., the semiconductor industry's leading supplier of factory automation software for Smart Manufacturing and Industry 4.0. Doug focuses on big data and remote connectivity solutions that help manufacturers collaborate securely on tools and data in production environments. A passionate advocate for Smart Manufacturing, Doug serves as an active member of the SEMI® Smart Manufacturing Advisory Council and Smart Manufacturing SIG, Americas Chapter.

Doug has over 20 years of experience leading software teams for a variety of industries including semiconductor, manufacturing, and transportation. Most recently, he was involved in architecting PEER Group's remote connectivity solution, Remicus™, and he was a champion in promoting the use of cloud computing and latest-generation web technologies.

Liquid system component cleanliness testing at 20 nanometres

D. Green
Applications Engineer
Particle Measuring Systems, Boulder, United States

Abstract

Fluid handling components such as valves, pumps, filters and degassing modules are common sources of contamination in high purity liquid distribution systems. This contamination can eventually reach the processing environment either in the form of solid particulates or, through chemical reactions, as a form of ionic contamination. Due to the significant cost associated with yield impacts, it is of vital importance to ensure that fluid handling components are sufficiently clean before they are used in the production environment. A simple testing program has been established that uses an optical particle counter to characterize the initial and long-term cleanliness of critical fluid handling components for particle sizes down to 20 nanometres. The testing program allows the relative cleanliness of components constructed out of different materials and from different manufacturers to be evaluated. This can save both time and money in the production environment by ensuring that the best components are selected for the designated task.

Biography

David Green graduated from University College London in 2002 with a bachelors degree in Physics. David has spent most of his career designing, building and testing novel particle analysis equipment. Since 2013 David has represented Particle Measuring Systems across the EMEA region as an Application Engineer.

Solutions for Process Matching and Monitory Using Wafer Based Metrology

T. Dupraz
SensArray European Business and Application Manager
KLA-Tencor, SensArray, Milpitas, United States

Abstract

In today's manufacturing environments there are increasing needs for in-situ monitoring of process tools' environments. Wafer process equipment manufacturers, IC manufacturers and reticle manufacturers use in-situ wafer-based sensor data to visualize, diagnose and control process conditions.
Whether you are developing a new process equipment, ramping a new 300mm manufacturing plant, implementing a new technology node in a 200mm line or increasing manufacturing productivity and efficiency, Wafer and Mask Based Metrology will provide unique feedback on your process.
Tool qualification, chamber matching, process monitoring and troubleshooting are some of the typical use cases that are enabled by KLA-Tencor's comprehensive portfolio of SensArray® products. With wired and wireless sensor wafers and reticles, automation solutions and data analysis systems, SensArray® products provide comprehensive information for a wide range of wafer and reticle processes.

Biography

Thierry Dupraz
KLA-Tencor
SensArray European Business & Application Manager
Thierry Dupraz has been working at KLA-Tencor since 1991, has filled technical, applications and management roles in KLA-Tencor's Defectivity & Metrology before joining the SensArray division in 2009 to cover and develop the European region business.

How New Macro Defect Inspection Technologies Are Becoming Essential to Increasing Yield and Reducing Wafer Fab's Costs

M. LaTorraca
Chief Marketing Officer
Microtronic, Inc., Hawthorne, NY, United States

Abstract
As semiconductors and intelligent devices are adopted into all areas of modern society it's critical that the inspection processes in manufacturing fabs keep pace.

Traditionally, semiconductor wafer manufacturers rely on sampling - at both the die and wafer level. Although sampling speeds up the inspection process, there is obvious risk of missing defective wafers due to sampling. While fabs will probably always rely on sampling to some extent, there are now new macro defect inspection applications that can be added to the wafer production environment to deliver dramatic improvements in many areas. These areas include: recipe-less defect detection; reduction of manual inspection costs; root cause analysis; shipping die with latent defects, excursion control, customer returns, and comprehensive automotive zero-defect strategy enablement.

This presentation focuses on why automated macro defect inspection is becoming essential to fabs as they are challenged to improve their quality in the already highly demanding semiconductor manufacturing environment. Exploding markets such as automotive and mobile devices make it necessary for fabs to provide better quality at lower costs.

For example, detection of macro defects in-line, prior to final inspection, allows manufacturers to take corrective action at an earlier, less expensive point in time to address any defective die and to prevent die with a high probability of carrying reliability defects, from entering customer products – including automotive devices. Additionally, automated macro defect inspection is ultra-fast and can inspect 3,000 wpd while delivering an actual high-resolution full-wafer color image. The macro defect inspection approach creates a complete, trackable "waferbase" with defect lists and defect maps along with each wafer's OCR number, image and slot position to help identify production problems fast and take corrective action quicker.

Biography
Mike LaTorraca is the Chief Marketing Officer of Microtronic, Inc., the US-based manufacturer of EagleView - the semiconductor industry's most yield enhancing macro defect inspection system and winner of the 2017 Semicon West Best of West new product of the year award.

Enhanced Fab productivity through powerful material flow automation

B. Stegemann
Sales Director
Fabmatics GmbH, Sales, Dresden, Germany

Abstract
We will deliver the content by e-mail to Mrs. Lidiia Timofeeva

Biography
Born in 1969, Burkhard Stegemann studied Physical Technics at the FH Aachen and completed his final year at Coventry University. In 1996 he joined Carl Zeiss in Jena in the department of microscopic wafer inspection. After two years in R&D/ application, he changed to product and project management. As part of the acquisition of the Zeiss business field “optical wafer inspection” by HSEB Dresden GmbH in 2004, Burkhard Stegemann joined HSEB. His responsibilities were sales and service. Since May 2014 Burkhard Stegemann is sales director of HAP GmbH Dresden and due to the merger of HAP and Roth & Rau - Ortner, since September 2016 sales director of Fabmatics GmbH.

Functional Semiconductor process tape ICROS ™ tape

A. Morimoto
Director
Mitsui Chemicals Tocello, Inc, R&D center,
Nagoya, Japan

Abstract

Mitsui Chemicals produces and supplies specialty chemicals and high performance polymers worldwide. We offer a broad range of Chemicals & Intermediates, Chemical Solvents, Specialty Polymers and Engineering Plastics, Functional Materials, Electronic Materials, and Adhesive Resins.

Regarding semiconductor manufacturing, Mitsui Chemicals Tocello provides a wide array of product lines featuring high-function adhesive tape such as Non-UV and UV surface protective tape used in silicon wafer back-grinding process, named ICROS ™ TAPE.

Today, ICROS ™ Tape is not only used for BG process but also for many other processes in semiconductor manufacturing flow, such as dicing, packaging process due to high functional technologies like heat resistant, chemical resistant property.

In his speech, Dr. Akimitsu Morimoto will present specific use case examples to outline how our tape technology helps to overcome the challenges related to precision process in semiconductor manufacturing and how manufacturers can benefit from these solutions.

Biography

Akimitsu Morimoto received his Ph.D in Chemistry from Tokyo Metropolitan University in 2003. Dr. Morimoto has worked for Mitsui Chemicals since 2003 and held various positions related to R&D, process engineering and applications support.

Currently, he is working as Director of R&D Group, Customer Support responsible for the company's global technical customer support organization.

Optimized Cu plating solution for next generation packaging

M. Hörburger
Global Product Manager Semiconductor Advanced Packaging
Atotech Deutschland GmbH, Semiconductor Advanced Packaging and Functional Electronics Coatings, Berlin, Germany

Abstract
Over the past years smartphones have become central to almost every aspect of our lives, which have increased the demand for high speed and reliable data connections. In order to handle these growing data capacity, the next generation smartphones and those equipped with 5G in particular will require even higher functionality and higher speed at shrinking component dimensions.
To cover this evolution, new technology solution, such as next generation RF filters are needed.

The presentation focus on a new requirement of two types of RF filters which is multilayer RDL with blind microvias and explain the challenges of Cu plating for this packaging technology.
Atotech has developed an new electrolytic Cu process that exactly addresses these challenges and offers a suitable solution for potential 5G applications.
.

Biography
Markus Hörburger received his diploma degree of business and chemistry from University of Ulm. He joined Atotech in 2014 and is in charge of the Semiconductor and Functional Electronic Coatings business as Global Product Manager.
In his function he is responsible for definition of R&D project's, integration / introduction and marketing related activities for Advanced Packaging, such as ECD (Pillar / RDL) and electroless (ENEPIG) processes respectively Functional Electronics Coating, such as products for Leadframe and Connector industry.

Before his actual position he worked at BASF as a Strategic Project Manager to bulit up an Innovation Network.

Solutions for processing SiC wafers and slicing SiC ingots with high speed and cost reduction

G. Klug
General Sales Manager
DISCO HI-TEC EUROPE, Sales Department,
Kirchheim b. München, Germany

DISCO
Kiru·Kezuru·Migaku Technologies

Abstract
DISCO Corporation is a leading manufacturer for equipment and tools for wafer thinning and dicing. Silicon carbide has become an alternative to Silicon when it comes to manufacturing high-power devices. However, singulating SiC wafers is challenging due to its hardness. The main challenge is maintaining high speed processing and best die quality at the same time. DISCO proposes suitable solutions for SiC processing with significant time and cost reduction and best quality. We introduce ultrasonic dicing and stealth laser for singulation and KABRA for ingot slicing. Processing SiC with standard dicing blade at a high speed causes chipping and cracks. Ultrasonic-wave dicing is a technology capable of reducing the processing load by applying ultrasonic vibrations in the blade radial direction. Lower processing load in ultrasonic-wave dicing enables the selection of a blade with smaller grit size improving the processing quality. SD is a technology that forms a modified layer by focusing a laser beam below the surface of a workpiece and then separating the workpiece into chips by breaking. SD is capable of processing SiC at a speed higher than that of ultrasonic-wave dicing, but both technologies prevent burr of metal layers and offer high die strength. So far, producing SiC wafers from an SiC ingot was a big cost issue, which hampered the development of SiC power devices. Slicing by wire saw requires a lot of time and is not cost-efficient. With KABRA, DISCO is introducing the new generation of SiC wafer production with high-speed ingot slicing. The KABRA slicing method forms a flat light-absorbing separation layer at a specific depth by irradiating a continuous, vertical laser from the upper surface of the SiC ingot. . By KABRA slicing, processing time is cut significantly while increasing the number of wafers per ingot. All of the above mentioned processes are offered by the Dicing-Grinding Service at DISCO HI-TEC EUROPE with its facilities close to Munich airport.

Biography
Gerald Klug studied business engineering at the University of Siegen and graduated in 1998 as Dipl.-Wirt.-Ing., completing his thesis at BMW in Munich. He started his career as a designer of coil processing lines for nearly 3 years at a German machine manufacturing company, Heinrich Georg GmbH. At the end of 2000, he joined DISCO as a Sales Engineer for the area of Scandinavia. Meanwhile he has been almost 18 years at DISCO, nowadays operating as General Sales Manager for the whole of Europe.

UBM Metallization Technology for advanced semiconductor devices

R. Preisser
Director Process Technology
AP&S International GmbH, Donaueschingen, Germany

Abstract
As semiconductor device geometries further shrink more devices migrate from wire bonding to flip chip technologies to overcome the technical limitations of the bonding technologies such as electrical resistance or the geometrical dimensions.

An under-bump metallization (UBM) is used as an alternative for the different options of device metallization such as Al-, Al-alloys and Cu to act as electrical contact, adhesion promoter and protection layer between this chip metallization and the following solder bump technology.

However the UBM deposition incl. pre- and post- treatment of the incoming wafers are critical to the interface stability and to reliability performance of the complete device. Some of this representative aspects has been evaluated, analyzed and assessed under different processing and/or test conditions using different material science and electrical test conditions.

Biography
CV Robert Preisser
Director Process Technology
AP&S International, Donaueschingen, Germany

• Started my professional career at IBM semiconductor development facility in Sindelfingen, Germany as process engineer with a chemical engineering background in 1974. Held several technical lead positions in various fields of SC technologies, including 3 technical R&D assignments (total of 5 years) to the IBM facilities in Burlington and Fishkill.

• Joint 1994 the semiconductor high purity chemistry division of Merck, Darmstadt, Germany as senior manager. Responsible for the development, build- and qualification- of high purity chemical supply units including the global high purity chemical service division

• 2012 joint Atotech, Berlin, Germany as VP- for the new established semiconductor metallization division. Founded and led for 4 years a new SC- chemistry research approach at CNSE in Albany, NY, USA. The approach included a R&D cooperation (2012) with Case Western Research University in Cleveland, OH for electrochemical research. Retired from Atotech in 2014.

• From 2014 until today part time adjunct professor at Case Western Research University in Cleveland and part time director for SC-processing technology at AP&S in Donaueschingen, Germany.

>100 publications in Semiconductor processing, SC- and MEMS- material development and application engineering.

Patents in SC-metallization technologies

SystematIC: Innovation in Integration

R. Visee
CEO
SystematIC Design B.V., Delft, Netherlands

Abstract
SystematIC designs and develops advanced custom IC's for sensor and power applications in the analog mixed signal domain. In SystematIC's products optical and magnetic circuits are often designed for a high voltage environment with low power requirements to the IC's. Trends we observe in the market are towards more integrated functionality, internal diagnosis and testability, minimum external component count at the lowest possible cost. Systematic circuit design techniques are applied in modern mixed signal CMOS IC processes for the product developments to excel in technical performance. Design for testability on waferprobe and final test are important requirements in the chip development. Lead frame customization leads to custom products in a standard assembly production lines. Examples of innovative products are presented in HV, optical and magnetic domain, as innovation in integration is advanced technology in actual products.

Biography
Richard Visée received his Electrical Engineering degree (MSc) at the Electronics department of the Technical University Delft. He proceeded to develop his skills in electronic design at the same department in a two-year in-depth study on the design of low-noise microphone amplifiers. After working as an analog design Engineer for three years, with a strong focus on RF circuit design, he joined SystematIC as a co-owner.
Besides working on many various IC design projects in sensor readout and power conversion, he developed SystematIC's Japanese business relations and now represents the company in projects for Japanese customers. He is also involved in collaborations with European research institutes and guides electronics development for space-related research.

MEMS and Semiconductor Applications for Wafers from Glass and Quarz

C. Seibert
Account Manager, Sales
Plan Optik AG, Sales, Elsoff, Germany

Abstract
Microelectromechanical systems (MEMS) and Sensors provide the magic that makes today's devices from our everyday life smart. MEMS consist of tiny mechanical and electrical devices such as membranes, mirrors and valves, as well as sensors, actuators and integrated circuits. Without MEMS or sensors, we would not have smartphones, smart homes and wearable smart watches, as well as a huge range of industrial and medical devices that require the functionality provided by MEMS and sensors.

This presentation will show different possibilities of using glass in MEMS and Semiconductor Industry, for example as glass carrier wafers, that enable handling and processing of ultra-thin semiconductor wafers that are needed to manufacture chips for smartphones and electronics.
Furthermore the use of glass wafers and dies in applications such as automotive lighting and sensing using wafer level packaging (WLP) technology will be shown as well as sneak peak into glass microfluidics and special applications for Silicon/glass compound wafers.

Biography
Christian Seibert is Sales Account Manager for Plan Optik AG, leading manufacturer for high quality wafers from glass, quartz and glass-Silicon.
At Plan Optik AG Christian is responsible for customers in US and Canada, helping them to find best wafer solutions and exceed requirements for their MEMS applications and Semiconductor processes.
Additionally he is working on product development for Plan Optiks' stock products and OTS (off the shelf) wafers as well as technical documentation.

Previous to this position Christian graduated as M. Eng. in Technical Sales from a dual study in cooperation between THM (Technische Hochschule Mittelhessen) and Plan Optik AG, working in Sales Department on establishing analysis and controlling of Sales.

Prior to that Christian finished his first dual study as B. Eng in Electrical Engineering in cooperation between THM and LTI Motion GmbH, provider of high dynamic and precision automation and drive solutions, working on various projects in departments such as application engineering, project- and product management and R&D.

Advances in doped AlN deposition techniques for next generation Piezo-MEMS

A. Barker
PVD Product Manager
SPTS Technologies Ltd, Newport, United Kingdom

Abstract

In BAW and Piezo-MEMS devices based on released membrane structures, AlN film stress state is of utmost importance and to maximise yield, manufacturers look to minimise stress variation across the wafer. When Sc is added to the film the problem becomes more demanding, as stress range tends to worsen with increased Sc content. Previous methods to control stress reach a limit of capability, impacting yield or compromising device design and performance. The problem is compounded when variations in Sc content exist in the film centre to edge, either as a result of chamber geometry, or sputter target homogeneity, impacting resonator film properties, such as coupling coefficient.

In addition to stress control, a related issue presents itself when Sc is added to an AlN film. During deposition, crystallites can form within the AlScN. Effectively defects in the film, the crystallite presence degrades resonator properties - dead volume amongst the piezoelectric bulk. Formation is abundant in areas of tensile stress, hence the relation to stress control. As with stress profile, crystallite density increases with Sc content so management of crystallite formation becomes another requirement for the PVD process, to ensure coupling coefficient yields are maximised.

In this paper we present a novel solution providing symmetrical control and adjustment of stress for AlN films with different Sc content, demonstrating excellent WIW stress performance, the ability to locally tune stress to compensate for centre to edge variations in Sc, and approaches to prevent formation of crystallite defects, maximising yield

Biography

Dr Anthony Barker joined Surface Technology Systems (STS) in 1997 as Etch Process Engineer. He went on to manage STS' non-Si based etch and deposition process groups. After leaving STS he joined Trikon as Etch Process Engineer in 2005, which became Aviza Technology and then merged with STS in 2009 to form SPTS Technologies. Most recently Anthony worked as Principal Process Engineer in R&D Accounts group before joining SPTS's PVD Product Management team in May 2017. Before STS, Anthony worked as Thin Film Process Engineer at Gems Sensors. Dr Barker has a B.Eng Honours degree in Materials Engineering and a Ph.D in Electronic Materials in association with Rolls Royce, both from Swansea University.

Innovations in photoresists and photopolymers for 2D / 3D micro and nano fabrication

A. Voigt
Business Unit Manager Photoresists
micro resist technology GmbH, Berlin, Germany

Abstract
Different methods for the manufacture of high resolution 2D and 3D features require a wide range of material solutions based on innovative photoresists and photopolymers. As a commercial resist supplier, micro resist technology aims at providing such solutions tailored for diverse lithography processes, comprising both materials and technology support. The following highlights will be presented:
E-beam lithography is a versatile patterning method for the generation of high resolution nano-patterns. Combining stepwise greyscale exposure and pattern reflow with a positive tone resist results in greyscale patterns of small dimensions.
Greyscale UV lithography of up to 100 micron thick resist films, either by direct laser writing or by conventional mask aligner exposure and a greyscale mask, can generate very deep greyscale micro-patterns. Both very thick films, and considerably smaller pattern features including sharp tips have been successfully fabricated using this technique.
Laser interference lithography is another method which allows the manufacture of nanoscale and periodic patterns even on very large substrates. Whereas two photon absorption (2PA) allows the generation of real 3D patterns at micro and nanoscale.
The development of photoresist and photopolymer materials tailored to meet the requirements of the specific technologies will be presented.

Biography
Anja Voigt received her diploma in 1993 and her PhD in 1998 in Photochemisty at the Humboldt-Universität zu Berlin. Since 1993 she has been a scientific co-worker with micro resist technology GmbH and responsible for R&D and production of negative photoresists. She has been the product manager for negative photoresists since 2005, and the business unit manager for photo resists at micro resist technology GmbH since 2012.