Materials Technology Session

J. Dekoster
Program Manager
imec, Leuven, Belgium

Biography
Johan Dekoster received the M.S. degree in Exact Sciences (Physics) in 1988 from the KU Leuven, Belgium. In 1993 he received the Ph.D. degree (Physics), also from the KU Leuven. From 1993 till 1999 he held postdoctoral fellowships from the Research Council and the Fund for Scientific Research at the Institute of Nuclear and Radiation Physics of the KU Leuven. In 1999 he joined the OTN business unit of Siemens. He was project leader for several hardware firmware development projects for data, voice, video and LAN. In 2007 he became program manager OTN at Nokia Siemens Networks. In April 2008 he joined imec as R&D manager of the Epitaxy group with responsibility on epitaxial deposition of group IV and III-V semiconductor materials. Since November 2012 he is program manager for equipment and materials suppliers collaborations at imec.

New conductors – What are the options for N5, N3 and beyond?

M. van der Veen
Senior Scientist Nanointerconnects Metallization
imec, Leuven, Belgium

Abstract
For several decades Cu, Al and W were used for interconnect wiring. Recently, due to resistance and reliability concerns alternatives to conventional conductors gained significant interest. Alternative metals are of interest to both memory and logic chips. In this talk imec's metal research activities will be showcased with a few implementation examples using damascene or subtractive processes. Benchmark to conventional conductors as well as future perspectives will be provided.

Biography
Marleen van der Veen is Senior Scientist and nano-interconnects metallization specialist. Marleen joined imec in 2008 with initial focus on graphene and Carbon NanoTubes synthesis, generating extensive experience on the growth and characterization of carbon-based materials (graphene, carbon nanotubes). As leading scientist in the EU project Technotubes and CARBonCHIP, she shifted to CNT integration for nano-interconnects. After her M.Sc. in. conducting polymers, she earned her PhD (2006) in organic chemistry and introduced pi-Logic systems for molecular interconnects. She continued as post-doc at Yale University electrical engineering to study surface plasma propagation in nanowires. She continues research at imec with a strong focus on new materials for advanced metallization schemes in nano-interconnects including the integration electrical characterization, and reliability aspects.

ALD/CVD applications, equipment and precursors in high volume manufacturing

J. Sundqvist
Group Leader
Fraunhofer IKTS, Thin Film Technology, System Integration and Technology Transfer, Dresden, Germany

Abstract

Research by Fraunhofer IKTS and TECHCET LLC, an advisory services firm providing electronic materials information, has shown that strong growth in IC fabrication demand for atomic-layer deposition (ALD), chemical-vapor deposition (CVD) should result in a combined global market size of US$1.3 billion by the year 2023. Metal precursors are expected to see a compound annual growth rate (CAGR) of 6.2 percent through 2023 starting from $460 million in revenues for this year. The market for dielectric materials is forecasted to be $465 million this year with CAGR of 8.2 percent through 2023, as detailed in the latest CMR. Plasma enhanced CVD and ALD processes drive increasing demand for silicon precursors, used in depositing the 32-72 layers and more of 3D-NAND chips and in self-aligned multiple patterning for advanced logic and memory chips. In addition, the research see a need for more advanced ALD/CVD precursor production in China, to support more leading-edge logic and memory fabs ramping production there. Cobalt (Co) metal is being used to encapsulate copper on-chip multi-level interconnects in the most advanced logic fabs for both foundries and IDMs. Intel is using full cobalt interconnects to replace some of the copper levels in its newest logic chips. The conservative demand forecast for cobalt metal in the form of ALD/CVD precursors for logic IC fabs is $25 million in 2018, with considerable growth to $70 million by 2023. Due to the competitive demand for cobalt needed for the lithium batteries used in EVs, and due to conflict issues in the supply-chain, cobalt metal pricing is volatile and reliable forecasting is correspondingly difficult. To anticipate supply-demand imbalances, the research also tracks ALD and CVD precursor demands in competing high volume manufacturing industries such as flat-panel display, photovoltaics, MEMS, and LED as well as emerging semiconductor ALD/CVD applications, equipment and precursor developments.

Biography

Jonas Sundqvist received his PhD in inorganic chemistry from Uppsala University, Department for Materials Chemistry at The Ångström Laboratory in 2003 where he developed ALD and CVD processes for metal oxide ALD and CVD processes using metal iodides. In 2003 he joined Infineon Memory Development Centre (MDC) as a process engineer for development of high-k and metal nitride ALD processes. Later at Qimonda (2006) he was a member of the Materials Management team for precursor procurement and acquisition with special focus on ALD precursors for DRAM development and production. In 2009 he joined Fraunhofer Center Nanoelectronic Technologies (CNT) as an expert for thin film deposition with special focus on high-k dielectrics and electrode materials for DRAM, eDRAM, BEOL MIM Cap and HKMG technologies. In 2010 he founded ALD Lab Dresden together with TU Dresden and in 2013 he became Group Leader of High-k Devices Group at Fraunhofer CNT which at the same time became a business unit of Fraunhofer IPMS. In 2014 Jonas foundSr. Technology Analyst of TECHCET— covers ALD and CVD precursors and related technologies, and is the co-chair of the Critical Materials Council (CMC) Conference. His over 20 years of work experience includes group leader of the High-k devices group at Fraunhofer's Center Nanoelectronic Technologies (CNT), which included 28nm node work for GLOBALFOUNDRIES Fab1. While there, he founded the ALD Lab Dresden together with TU Dresden. At Infineon Memory Development Centre (MDC) he developed high-k and metal nitride ALD processes, and at Qimonda he was a materials manager focused on the ALD / CVD precursors supply-chain. He is the founder of BALD Engineering, an independent blog and networking platform for ALD. He holds a Ph.D. and a M.S. in inorganic chemistry from Uppsala University, Sweden, a B.S. in electrical and electronics engineering from Lars Kagg, and nine patents.ed BALD Engineering AB, an independent Networking Platform for ALD. Since 2016 Jonas is leading the Thin Film Technology Group within the System Integration and Technology Transfer Department of Fraunhofer IKTS in Dresden Germany. He is also a part time Sr. Technology Analyst of TECHCET— covers ALD and

CVD precursors and related technologies, and is the co-chair of the annual Critical Materials Council (CMC) Conference.

Dr. Sundqvist has over 10 years experience, holds 10 patents and authored or co-authored more than 30 publications in the fields of ALD and CVD process development.

Advancing Atomic Layer Deposition and Atomic Layer Etching

H. Knoops
Atomic Scale Segment Specialist
Oxford Instruments Plasma Technology, Bristol, United Kingdom

Abstract
Atomic scale processes such as atomic layer deposition (ALD) and atomic layer etching (ALE) are increasing in popularity with more and more applications requiring or benefitting from atomic level control. ALD and ALE provide the control they do because they are based on self-limiting surface processes. This contribution will discuss the basics for both techniques and discuss how they can be further advanced.

For ALD two trends will be discussed: i) controlling the ion energy in plasma ALD to tune material properties. Generally processes are optimized to have minimal ion energies to avoid potential damage. Interestingly, for these low damage plasma sources, the ion energy can be increased by substrate biasing providing additional knobs for tuning film properties. Key examples are stress-control of oxides such as achieving near-zero stress in TiO_2 and reduction of the resistivity of conductive nitrides (e.g. for TiN, HfN_x, and NbN). ii) Usage of novel plasma gases. For instance H_2S plasma gas mixtures have been shown to allow growth of 2D-MoS_2 at low temperatures and SF_6 plasma was found to allow ALD of AlF_3, which could be of interest as an optical coating or for batteries.

For ALE the basics will be discussed and how these can be used for applications. More and more processes are being developed (e.g. ALE of GaN, AlGaN, Si, SiO_2 & 2D materials). Interestingly besides the exact control of etch depth, other aspects of ALE might turn out to be more important for certain applications. For instance ALE of AlGaN was found to reduce the surface roughness, while generally plasma etching would increase the surface roughness somewhat. Other advances for both ALD and ALE are expected to be in the form of combinations with other techniques. Therefore clustering of ALD and ALE tools with 2D materials growth can allow precise control of interfaces and allow avenues into selective growth, surface cleaning and etching.

Biography
Dr.ir. Harm Knoops is an Atomic Scale Segment Specialist for Oxford Instruments Plasma Technology (OIPT) and holds a part-time assistant professorship position at the Eindhoven University of Technology. His work covers the fields of (plasma-based) synthesis of thin films, advanced diagnostics and understanding and developing plasma ALD and similar techniques. His main goals are to improve and advance ALD processes and applications for Oxford Instruments and its customers. He has authored and co-authored more than 40 technical papers in peer-reviewed journals.

Atomic layer deposition for the synthesis and integration of 2D materials for nanoelectronics

A. A. Bol
Associate Professor
Eindhoven University of Technology, Applied Physics, Eindhoven, Netherlands

Abstract

Graphene and other layered 2D materials have been the focus of intense research in the last decade due to their unique physical and chemical properties. This presentation will highlight our recent progress on the synthesis and integration of 2D materials for nanoelectronics applications using atomic layer deposition (ALD). ALD is a chemical process that is based on self-limiting surface reactions and results in ultrathin films, with sub-nm control over the thickness and wafer-scale uniformity. Two of the critical issues in unlocking the potential of graphene are the ability to deposit ultra-thin high-K dielectrics on grapene and fabricate low resistance contacts to graphene. Technologically, it is desirable to use atomic layer deposition (ALD) for this purpose. The inert nature of graphene however has made ALD on graphene very challenging. This presentation will give an overview of ALD techniques that were developed in our lab to initiate oxide and metal ALD on graphene to form ultrathin dielectrics and low-resistance contacts, without deteriorating graphene's electrical properties.

In addition, ALD might prove as a key enabler for tackling the current challenge of large-area growth of 2-D materials with wafer level uniformity and digital thickness controllability. We have implemented plasma-enhanced ALD to synthesize large-area MoS_2 thin films with tuneable morphologies i.e. in-plane and vertically standing nano-scale architectures on CMOS compatible SiO_2/Si substrates. The large scale 2D in-plane morphology has potential applications in nanoelectronics, while the 3D nanofin structures could be ideal for catalysis applications such as water splitting.

Biography

Ageeth Bol is associate professor of Applied Physics at Eindhoven University of Technology, the Netherlands. She received her MSc and PhD in Chemistry from Utrecht University, the Netherlands. After obtaining her PhD degree in 2001 she worked for Philips Electronics and at the IBM TJ Watson Research Center in the USA. In 2011 she joined the faculty of Eindhoven University of Technology. In 2012 she received a prestigious VIDI grant from the NWO (Netherlands Organization for Scientific Research) and in 2015 she was awarded a Consolidator Grant by the ERC (European Research Council). Her current research interests include the fabrication, modification and integration of 1-D and 2-D nanomaterials for nanodevice applications and catalysis.

Innovative Compound Semiconductor Based Engineered Substrates for Photonics, Power, Solar and RF Applications

E. Guiot
Product Development Manager
Soitec, Bernin, France

Abstract

The Smart Cut ™ technology applied to the fabrication of SOI, is used in volume manufacturing by SOITEC, serving digital, RF, power and photonics markets. Application of this technology using ion implantation to transfer thin films of compounds semiconductors has also been developed. The Smart Cut ™ process has technical and economical advantages. Transfer of thin layers onto many various materials with both a good thickness homogeneity and a high crystalline quality has been demonstrated. From an economic point of view, the possibility of reusing the remainder of the implanted substrate helps to reduce costs, especially for the III-V materials. We will focus on the application of the Smart Cut ™ technology for two different materials, InP and GaN.

InP is widely used for the optoelectronic market. The Smart Cut ™ technology, has been tuned to this material. In addition to the cost advantage of the recycling, different receiver substrates such as GaAs, Sapphire or Si have been evaluated to enable new functions: receiver lift off, lower fragility, better integration. Using the InP-on-GaAs engineered substrate combined with direct wafer bonding, Soitec together with Fraunhofer ISE and CEA Leti have demonstrated wafer bonded 4-junction solar cells with highest conversion efficiency of 46.1 %. We will discuss also how the Smart Cut™ technology can enable the use of InP for RF 5G products.

Regarding GaN, Smart Cut ™ technology enables the layer transfer of up to 1 µm thick GaN films either from bulk GaN or GaN on sapphire. We have demonstrated up to 3 cycles of reuse of the GaN donor substrate. Different receiver substrates such as Sapphire, Molybdenum and polycrystalline Aluminum Nitride have been evaluated. Through this innovative engineered GaN substrate, we have demonstrated a 20µm GaN epi growth. This breakthrough could enable new vertical GaN devices for high power application such as electric vehicle powertrain and RF power products serving the 5G market.

Biography

Dr. Eric Guiot, Materials Science Doctor (Ph.D. from Paris University, Pierre et Marie Curie), now is product development manager for compound semiconductors in Soitec. He is graduated from the Ecole Centrale engineering school in France. He made his PhD on the development of epitaxy of iron oxide targeting giant magnetoresistance materials. He then joined Corning Fontainebleau Research Center in France for the development of integrated optics devices for telecommunication. In 2002 he joined Soitec in France. He has been working on the development of advanced engineered substrates targeting various applications covering digital application at advanced nodes and optoelectronics. He is now leading the product development group focused on compound semiconductor engineered substrates targeting power, solar, photonics and RF application.

Kokusai Electric Corporation new products offering for 2018

Y. Kitahara
New Products offereing as Kokusai Electric
Kokusai Semiconductor Europe GmbH, President & Managing Director, Erkrath, Germany

Abstract

1)Increasing Risk on Obsolete Parts: customers are suffering the risk of manufacturing discontinuity attributed to parts supply obsoleting. So they must realize some solution to secure their uninterrupted chip supply for Automotive, preferably by upgrading their existing aged installed bases but less likely because already some parts obsoleted.

2)Statistical data set requested to submit and store by Automotive OEM: Since Automotive OEMs must secure reliability for Autonomous & Connected car, so they request our customer to provide statistical data of process parametric but most of aged equipment can't do parametric data collection, but Kokusai can.

3)Limited footprint/height restriction allowed to use: To minimize CAPEX, customer try to replace current aged equipment with renovated models, but SPE OEMs must meet given space/height restriction as it is. As most of renovated tools were designed based on 300mm platform, so likely to need more space and higher ceiling height, besides Kokusai.

4)Latest process technology required for IoT Module chipsets: latest technical paper related to IoT based chips need both older process like POCl3 and modern process like Al2O3 or relevant material. As an example, MEMS Si Oscillator has > 170C thermal budget but Crystal Oscillator not. MEMS Oscillator may require > 5E20 ions/cm3 high P dosed Si layer then now reconsidering use of POCl3 to satisfy such device spec. Also, some MEMS actuator or interlayer Hi-k MIM caps may require Al2O3 and PZT layer or relevant. Since customer need to suppress leak current to be < 1E-8A/cm2 while achieving >10fF/um2 capacitance which likely self-contradictory, so sophisticated tuning and right choice of oxidizer is mandatory as Kokusai did.

Biography

Yoshio Joe Kitahara, graduated from St. Paul's Univ. studying on Statics as Mathematics and joined TEL in 1983 and spent 8 years long both at Japan and Bay Area/SFO primarily doing new product research in Silicon Valley. As a next, joined AMAT starting from Product Marketing job for Endura PVD and went through various products in charge(CVD/Etch/CMP/Inspection & Metrology/Mask production equipment). Since 2011, joined MEMC as Sales GM for Japan, also from 2011, joined Kokusai Electric (former Hitachi Kokusai Electric) as GM of Product Development Planning and Marketing. Since 2017 he became President & Managing Director of Kokusai Semiconductor Europe to date.