Fraunhofer Demo Day

J. Pelka
Managing Director
Fraunhofer Group for Microelectronics, Berlin, Germany

Biography

Dr. Joachim Pelka is the Managing Director of the business office for the Fraunhofer Group for Microelectronics. He studied electrical engineering, with an emphasis on semiconductor technology, at Berlin's Technical University and was awarded a doctorate there for his work on semiconductor components. He has been with the Fraunhofer-Gesellschaft since 1983.

Today, following many years in the organization, Dr. Pelka is the Managing Director of the Fraunhofer Group for Microelectronics. His previous position was as the Fraunhofer ISIT's department head responsible for the simulation of semiconductor patterning processes. He also spent two years in the JESSI coordination office (also located at the ISIT). As managing director he is responsible for strategic planning and for the coordination of work in the microelectronic institutes of the Fraunhofer-Gesellschaft.

Under his directorship, the business office carries out studies on current areas of research that form the basis for the Group's strategic planning. In the past, this included for example the "MST fireside chats", a series of workshops conducted on behalf of the project sponsor, Mikrosystemtechnik VDI/VDE IT and a study concerning road mapping activities of microelectronics on behalf of the CATRENE Scientific Committee.

In keeping with deepening European integration, Dr. Pelka today functions more and more as a contact person for other European research facilities such as CEA-Leti, CSEM, IMEC and VTT. He represents the Group, complementing the Chairman of the Group, in the Heterogeneous Technology Alliance HTA.

Dr. Pelka is a member of the ENI2 Steering Committee and the organizational committee of the INC Conference Series. The International Nanotechnology Conference on Communications and Cooperation INC9 held in Berlin in 2012 was organized under his supervision. Currently, he has been focusing on a study named "smart cities" commissioned by the CATRENE Scientific Committee.

3D Wafer Level System Integration

M.J. Wolf
Head of Department
Fraunhofer Institute for Reliability and Microintegration IZM, Berlin, Germany

Abstract

3D integration is considered to be the key technology in microelectronic packaging to meet the requirements of future electronic systems especially with respect to the integration of even more functions, miniaturization, performance, energy efficiency. According to these increasing application driven demands System in Packages (SiP) using 3D integration are key elements for advanced microelectronic packaging. The heterogeneous integration of different devices by using 3D architectures allows the realization of applications especially optimized for SiP in a high efficient and cost effective way. Key elements for 3D wafer level SiPs are the formation of Through Silicon Vias (TSVs) and their process integration into active devices as well as silicon interposer as a key enabler for 3D Systems which are very attractive to deal with system performance

improvement and to achieve cost effective packaging solutions.
To meet the complexity of this technological approach, five Fraunhofer Institutes cluster their competencies in a network to cover a broad spectrum of topics related to 3D integration. The presentation will show the complex correlation of the different aspects of 3D integration covering the fields of technology, design and reliability.

Biography
M. Juergen Wolf received a M.S. degree in Electrical Engineering. In 1994, M. Juergen joined Fraunhofer Institute for Reliability and Microintegration (IZM), Berlin and has worked e.g. as group & project manager in the field of wafer level packaging and system in package (SiP). Since 2011 he is head of department Wafer Level System Integration, responsible for the coordination and management of ASSID - "All Silicon System Integration Dresden-ASSID" with its 300 mm Wafer Level Integration. He manages as well as participates in a number of research projects on European and international level. M. Juergen Wolf is a European representative in the technical working group Assembly & Packaging of ITRS, JEC, JIC and a board member of EURIPIDES as well as member of IEEE and SMTA. He is also chair of Fraunhofer Cluster 3D Integration. He has authored and co-authored numerous scientific papers and reports in the field of microelectronic packaging and holds a number of patents.

Physical Failure Analysis at 3D Structure

E. Zschech
Director of Materials and Nanoanalysis Division
Fraunhofer Institute for Ceramic Technologies and Systems IKTS, Dresden, Germany

Abstract
- TBA -

Biography
Ehrenfried Zschech is Director of Materials and Nanoanalysis Division at Fraunhofer Institute for Ceramic Technologies and Systems IKTS in Dresden, which he joined in 2009. He received his diploma degree in solid-state physics and his Dr. rer. nat. degree from Dresden University of Technology. After having spent four years as a project leader in the field of metal physics and reliability of microelectronics interconnects at Research Institute of Nonferrous Metals in Freiberg, he was appointed as a university teacher for ceramic materials at Freiberg University of Technology. In 1992, he joined the development department at Airbus in Bremen. There he managed the metal physics group and worked on laser-joining metallurgy of light metals. From 1997 to 2009, Ehrenfried Zschech managed the Materials Analysis Department and the Center for Complex Analysis at AMD in Dresden. In this position, he was responsible for the analytical support for process control and technology development, as well as physical failure analysis. His current research interests are in the areas nanomaterials and nanoanalysis, with the focus on thin film technology and nanotechnology. He has published three books and more than 170 papers in scientific journals in the areas of solid-state physics, materials science and reliability engineering. He holds honorary professorships for Nanomaterials at the Brandenburg University of Technology in Cottbus-Senftenberg and for Nanoanalysis at the Dresden University of Technology. Ehrenfried Zschech is acting as Past President of the Federation of European Materials Societies (FEMS).

Ultra-thin capacitors for enabling miniaturized IoT applications

K. Seidel
High-key Devices
Fraunhofer Institute for Photonic Microsystems IPMS, Dresden, Germany

Abstract
The growing demand on small system solutions for internet of things applications is driving the compression of many functions into small package outline. This also requires sophisticated solutions for the integration of passive components in order to avoid external circuitry. In many cases it is required to suppress cross-coupling between different power planes. That can be achieved by placing decoupling capacitors as close as possible to the circuits.
The demonstrator that was developed in joint collaboration between Fraunhofer IPMS-CNT and Fraunhofer IZM-ASSID presents a very compact and thin capacitor for direct integration into chip-package. The capacitor concept can be easily adjusted regarding design and electrical properties to the requirements of customers. A wide range of capacitance values from pF to µF in a small footprint is achieved by means of high-k material integration and special patterning processes, thus supporting a broad application range from RF-filtering to decoupling and energy buffering. Based on characterization results of voltage and temperature characteristics it is shown that this concept offers good electrical properties and linearity compared to conventional ceramic capacitors, like MLCC.
Besides the integration in chip package (System in Package) this capacitor solution is suitable for embedding in high-end PCB as well. Furthermore this modular capacitor fabrication concept can be applied within chip-interconnect metallization levels or on interposers.

Biography
Konrad Seidel received the Diploma degree in electrical engineering from the Dresden University of Technology, Germany, in 2003.
From 2004 to 2008, he was with the Reliability and Qualification team of Flash Product Engineering, Infineon Technologies AG, Dresden, Germany, later Qimonda.
Since 2008, has been working as research associate with Fraunhofer Center Nanoelectronic Technologies, Dresden, which is now a business unit of Fraunhofer Institute for Photonic Microsystems, Fraunhofer IPMS. His research focus areas are electrical characterization and reliability of integrated circuits as well as the integration and design of integrated high density capacitors.

High Temperature 0.35µm SOI CMOS Process (250°C and beyond)

S. Dreiner
Group Manager/Deputy Head of Department
Fraunhofer Institute for Microelectronic Circuits and Systems IMS, Duisburg, Germany

Abstract
The application temperature of microelectronic circuits has been steadily increasing over the years (125°C-> 150°C-> 175°C) and will be even higher in the next future. This is due to new challenges regarding energy efficiency, reduction of emissions and reduction of system size, for example in the automotive and aviation markets. The exploration of natural energy resources (gas, oil, geothermal) is a high tech operation with sophisticated sensor and data acquisition systems that are among the core technologies to enable deep hole drilling (T>200°C). The recent availability of power devices based on GaN and SiC in combination with a high temperature capable CMOS (for control electronics) offer the potential for making significant progress since driver and power device can operate at temperatures beyond 200°C, increasing overall system efficiency and drastically reducing cooling effort and package size.
Published work on high temperature CMOS circuits typically refers to technologies with a minimum feature size of 0.8 to 1.0 micron even though for complex digital circuits this results in large die size. Technologies with smaller feature size are available but typically not suitable for reliable high temperature (>175°C) operation due to high leakage, decreasing threshold voltages over temperature or reliability issues with the standard aluminum metallization.
Fraunhofer IMS has developed a high temperature 0.35 micron thin film SOI CMOS technology. The mixed signal technology provides numerous devices, e.g. specific transistors for analog and digital domain, diodes, resistors and voltage independent capacitors. Also non-volatile memory cells (EEPROM) are available. In addition the technology is equipped with a tungsten metallization for highly reliable operation even at high temperatures.
An overview on the new technology including characterization results of devices and test circuits is given in the presentation.

Biography
Dr. Stefan Dreiner studied Physics at the University of Essen/Germany and graduated with Diploma degree in 1996. He received the Ph.D. degree in physics from the University of Münster/Germany in 2002. Afterward, he was a Postdoctoral Fellow with the Technical University of Dortmund/Germany. Since 2005, he is with Fraunhofer Institute for Microelectronic Circuits and Systems, Duisburg, where he is currently Manager of the Semiconductor Processes and Devices Group. Focus of his group is the CMOS technology and devices development for special purposes like high temperature (high voltage) and the integration of optical and other sensors in CMOS.

Integrated Micro Camera Devices

M. Töpper
Business Unit Developer
Fraunhofer Institute for Reliability and Microintegration IZM, Berlin, Germany

Abstract
Packaging is a dominant part for the integration of image sensors into electronic systems for ultra-small and/or high performance applications. This live presentation will focus on the packaging and system integration aspect of image sensors. Two different approaches will be presented and discussed in detail: One approach is a wafer level packaging concept using TSV (Through Silicon Vias) technology and the other is an image sensor on a small PCB with embedded image processor. Both technologies are a versatile step for new and advanced systems.
The enabling key technology for wafer level packaging of camera systems based on top-side illuminated imagers are TSV because they allow a redistribution on the backside of the wafer wherefore the active side remains unaffected and can be completely used for the optic assembly. The wafer level camera having a size of about 1mm x 1mm will be presented in a live-demo.
Another packaging process was made possible by an embedding technology. At a size of only 16x16x12 cubic millimeters, including, the microcamera module is an extremely small system. A total of 72 passive and 13 active components (such as oscillators, DC-to-DC converters, memory chip and image processor) have been embedded inside the module and the image sensor is mounted on top. The main system advantage is the fact that the image material is directly inside the camera, since it is equipped with an integrated processor for image processing. In addition it is fully encapsulated. After the image sensor has recorded the image, the integrated processor evaluates the frame. The video itself no longer has to be sorted and analyzed by an interposing system. Instead, only the relevant signals are transmitted. This camera will be also demonstrated.
An outlook on a crowd-funding project will be given leading to the next step of integration. Based on an universal and flexible programmable image sensor SoC developed by Fraunhofer IIS/EAS a new "SmartHighProCAM" will be developed in cooperation with Fraunhofer IZM.

Biography
Michael Töpper has a M.S. degree in Chemistry and a PhD in Material Science. Since 1994 he is with the Packaging Research Team at TU Berlin and Fraunhofer IZM. In 1997 he became head of a research group. In 2006 he was also a Research Associate Professor of Electrical and Computer Engineering at the University of Utah, Salt Lake City. The focus of his work was Wafer Level Packaging applications with a focus on materials. Since 2015 he is part of the business development team at Fraunhofer IZM. Michael Töpper is Senior Member of IEEE-CPMT and has received the European Semi-Award in 2007 for WLP. He has published several book chapters and is author and co-author of over 200 publications.

Cost efficient miniaturised silicon micropumps

M. Richter
Head of Department Micromechanics, Actuators and Fluidics
Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT, Munich, Germany

Abstract
Silicon MEMS components require high number of pieces for efficient manufacturing. On the other side, the manufacturing costs of high volume applications for MEMS components in automotive, consumer (like smart phone industry), and disposable drug delivery applications has to be very low, most of it in the region below 1$ / component and below.

Due to physical reasons, MEMS actuators like silicon micropumps require a certain chip size to meet functional challenges like back pressure, compression ratio, and flow rate. The smallest state of the arte micropumps are made of Silicon (e.g. chip sizes: Fraunhofer micropump 7x7 mm2, Debiotech micropump: 6x10 mm2). That chip size makes it very difficult to meet manufacturing costs mentioned above.

It is evident that manufacturing cost scale down with the chip size of the silicon micropump. With that, to address high volume applications it is essential to shrink the micropump chip furthermore. On the other side, it is just difficult to meet micropump performance parameters like stroke volume, flow rate, compression ratio or back pressure ability, if just the lateral dimensions of the actuation diaphragm will be reduced. Next, not only the silicon front end technology, also the back end manufacturing steps like piezo mounting has to be cost efficient. Finally, also the fluidic test cost of the micropump chip.

In this presentation an overall strategy will be presented for a Technology platform for Silicon micropumps with small chip sizes down to 3x3 mm2. Results of this strategy regarding piezo mounting on wafer level, fluidic micropump test on wafer level are explained.

Finally, first performance results of a 5x5mm2 micropump chip will be presented.

Biography
Martin Richter´s mission is to enable microdosing systems for industrial applications. He completed his studies in technical physics at the Technical University of Munich, and gained his PhD at the University of Armed Forces in the area of microfluidics.
Since 2000 he has been heading the department Micromechanics, Actuators and Fluidics at Fraunhofer. His scientific focus is on microfluidic actuators such as micro pumps, micro valves, open jet dispensers or micro blenders, and integrating these in microfluidic systems.
Such microfluidic actuators are deployed in varied applications, e.g. in medical technology (such as drug dosage, glaucoma therapy), laboratory technology or dosage of lubricants.

Advanced Sensor Technologies

J. Amelung
MEMS Business Manager
Fraunhofer Institute for Photonic Microsystems IPMS, Dresden, Germany

Abstract
- TBA -

Biography
- TBA -

GMR based 2D magnetic field sensors

P. Matthes
Head of magnetic sensor technology group
Fraunhofer Institute for Electronic Nano Systems ENAS, Chemnitz, Germany

Abstract
Magnetic field sensors have been utilized for various applications such as, for instance, switches, positioning and velocity sensors, ampere meters or can even be used as a weighing device. Most commercially available sensors are based on the anisotropic magnetoresistance (AMR) effect or the Hall effect, both being robust and allowing, e.g., angular as well as very high field sensitivities. Even higher field sensitivities are expected for giant magnetoresistance (GMR) or tunneling magnetoresistance (TMR) effect based sensors, which, furthermore, can be less power consumable and scaled to smaller dimension.
We have designed and studied 2D GMR spin valve sensors (IrMn/CoFe/Cu/CoFe/NiFe) in monolithic integration for high sensitivity applications. For a maximum signal-to-noise ratio we realized a focused double Wheatstone bridge layout, featuring an antiparallel exchange bias pinning for neighboring meanders and an orthogonal pinning for different bridges. This precise alignment is achieved with microscopic precision by local ns-laser heating and subsequent in-field cooling.
Striving for maximum signal sensitivity and minimum hysteresis, we studied the impact of single meander geometries (e.g. stripe width, stripe length) and different alignments of the locally defined reference magnetization with respect to the meander stripes on the electronic transport properties. Using a set of optimum parameters, we demonstrate that our sensor may readily be employed to measure small magnetic fields, such as the ambient (geomagnetic) field, in terms of a 2D vector with high spatial (~200 µm) and temporal (~1 ms) resolution.

Biography
Patrick Matthes started to study physics at the Chemnitz University of Technology in 2005. In his diploma thesis he investigated the magnetic properties of FePt thin films deposited on previously optimized MgO and Cr seed layers. After his diploma in 2010 he continued as a PhD student in the group of Prof. Albrecht and since July 2015 he is head of the magnetic sensor technology group at Fraunhofer ENAS. His research activities concentrate on coupling phenomena and magnetic as well as magneto-transport properties of magnetic thin films and nanopatterns.

SEEDs - intelligent use of energy in small and medium-sized companies

R. Öchsner
Division Director
Fraunhofer Institute for Integrated Systems and Device Technology IISB, Erlangen, Germany

Abstract
- TBA -

Biography
- TBA -

Bearing with integrated Energy and Data Transmission

T. Heckel
Research Fellow
Fraunhofer Institute for Integrated Systems and Device Technology IISB, Erlangen, Germany

Abstract
The ability to transfer power in fast rotating systems is required for a wide range of applications, such as wind power systems with electronics integrated in the rotor blades or highly-automated Industry 4.0 production platforms. In this talk, a technology for the contactless transfer of power and data in fast rotating objects using the example of a standardized ball bearing is presented. This alternative to failure-prone cable-based solutions like slip rings offers further advantages such as improved safety for manufacturing systems, the chemical industry, and medical technologies. The bidirectional data transfer offers both system safety functions as well as an interface for sensors and machine controls. This contribution is supported by the Bavarian Ministry of Economic Affairs and Media, Energy and Technology as a part of the Bavarian project "Leistungszentrum Elektroniksysteme (LZE)".

Biography
Thomas Heckel studied Mechatronics focussing on power electronics, control theory, and drive technologies. He received the Diploma degree from the Friedrich-Alexander-University Erlangen-Nuremberg, Germany, in 2011. Since then, he has been working at Fraunhofer IISB and the Chair of Electron Devices, Erlangen, on his Ph.D. thesis. His research interests include the characterization and application of Wide-bandgap semiconductors in high efficiency power electronics as well as inductive power transfer systems. Furthermore, he is currently project manager of one of the pilot projects of the "Leistungszentrum Elektroniksysteme" in Erlangen.

Energy-independent asset tracking system for logistic applications

H. Milosiu
Senior Engineer RF- and Microwave IC-Design
Fraunhofer Instiute for Integrated Circuits IIS, Erlangen, Germany

Abstract
Energy-independent extremely efficient sensor nodes are one of the key technologies for the "Green Internet of Things" and "Smart Objects".

Thereby, a sub-10-µA UHF WakeUp receiver plays a central role. Pursueing a high-performance logistics solution, this project involves the implementation of an asset tracking system, including the development of the electronics for the gateways and location beacons, as well as a miniaturized wireless tag integrated into the tracked asset. An energy-saving wireless solution is especially important for this application. The tag electronics consist of a three-band wake-up receiver with a current consumption below 10 µA, plus an efficient UHF two-band transmitter. The tag will be completely powered with energy harvesting technology for permanent autonomous operation. The energy-saving electronics solutions developed in this project will be suitable for a wide range of applications such as logistics, building automation, intelligent lighting, electronic labels, remote maintenance and control and wireless sensor networks.

Biography
Heinrich Milosiu was born in Regensburg, Germany, in 1976. He received the Masters degree in electrical engineering from the Friedrich-Alexander-University of Erlangen-Nürnberg, Germany, in 2002, and the doctoral degree (Dr.-Ing.) in 2012.
He has been with Fraunhofer Institute for Integrated Circuits (IIS) in Erlangen since 2002. His research interests are RF CMOS synthesizer design and UHF receiver design in the sub-10 microwatts area. Since 2008, Dr. Milosiu has been project manager for UHF Wake-Up Receiver Design. Dr. Milosiu has been lecturer at the Friedrich-Alexander-University of Erlangen-Nürnberg since 2014.